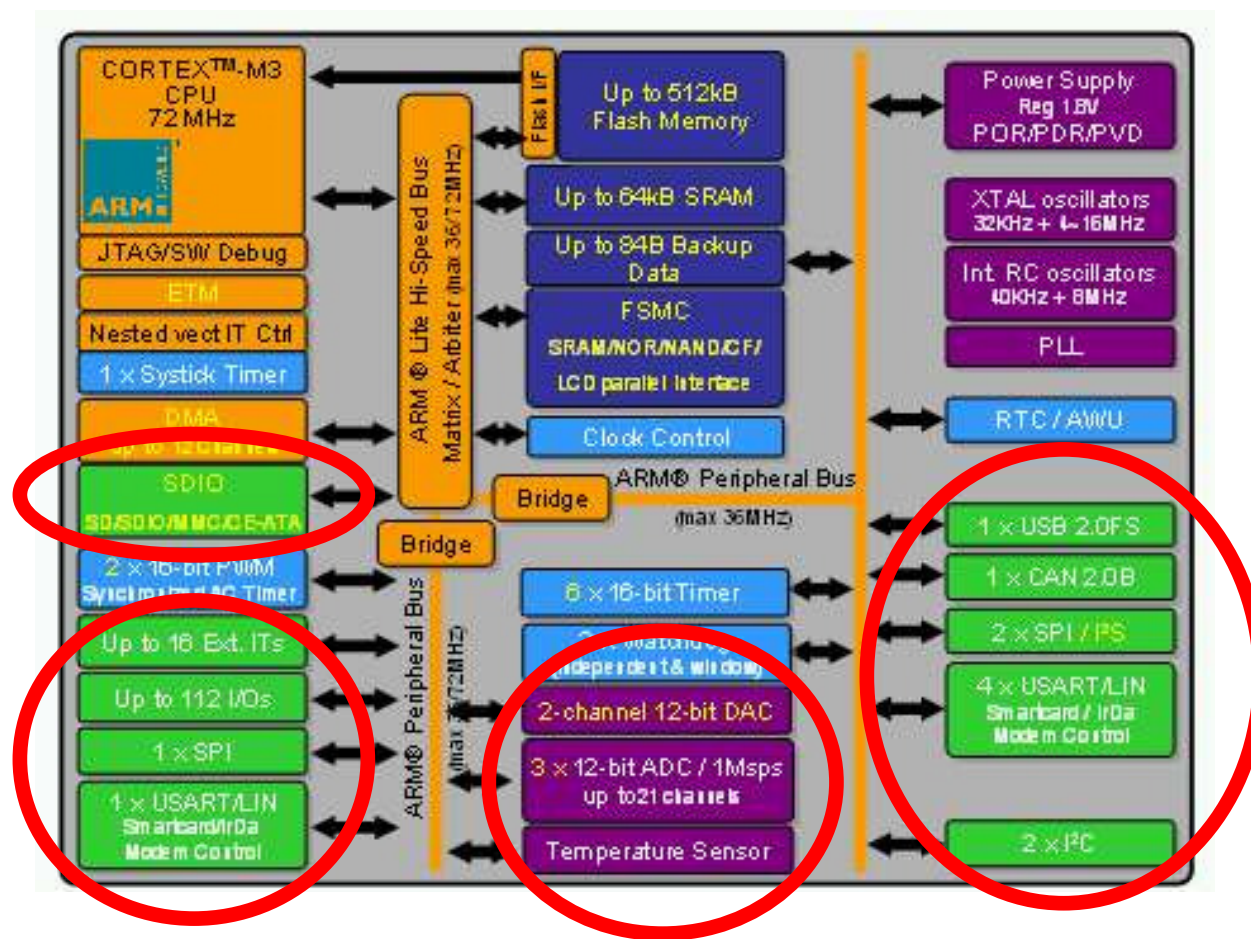


Microcontrollori – Periferiche Interne



Microcontrollori – Periferiche Interne

Peripherals registers

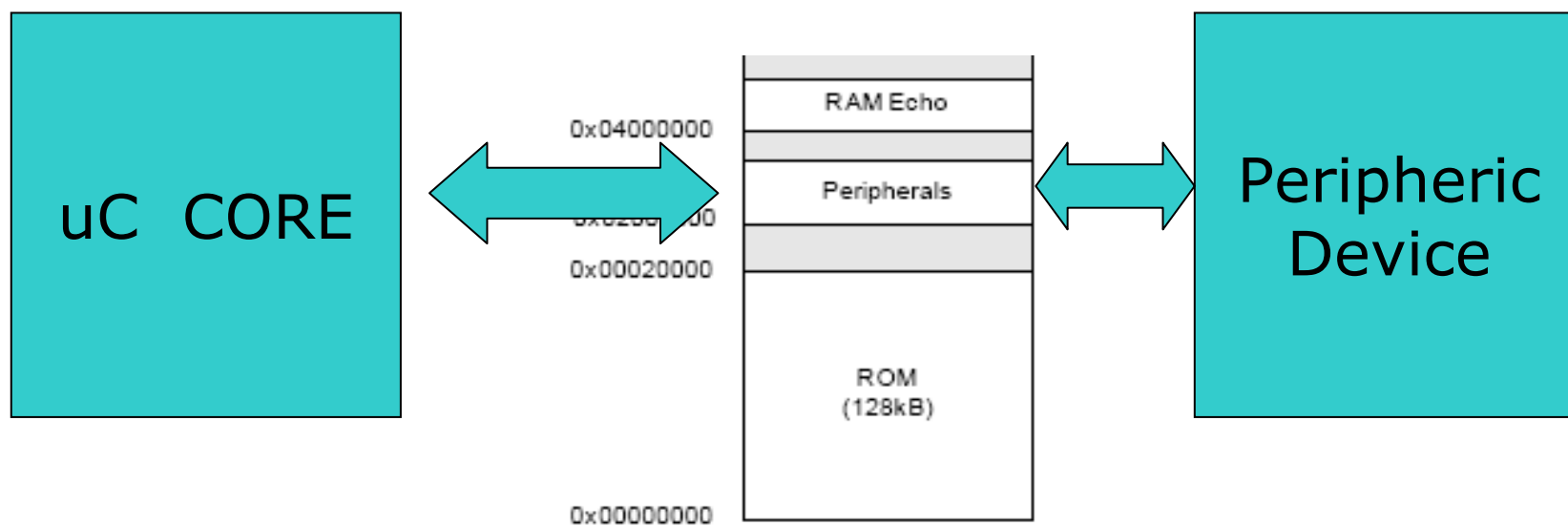
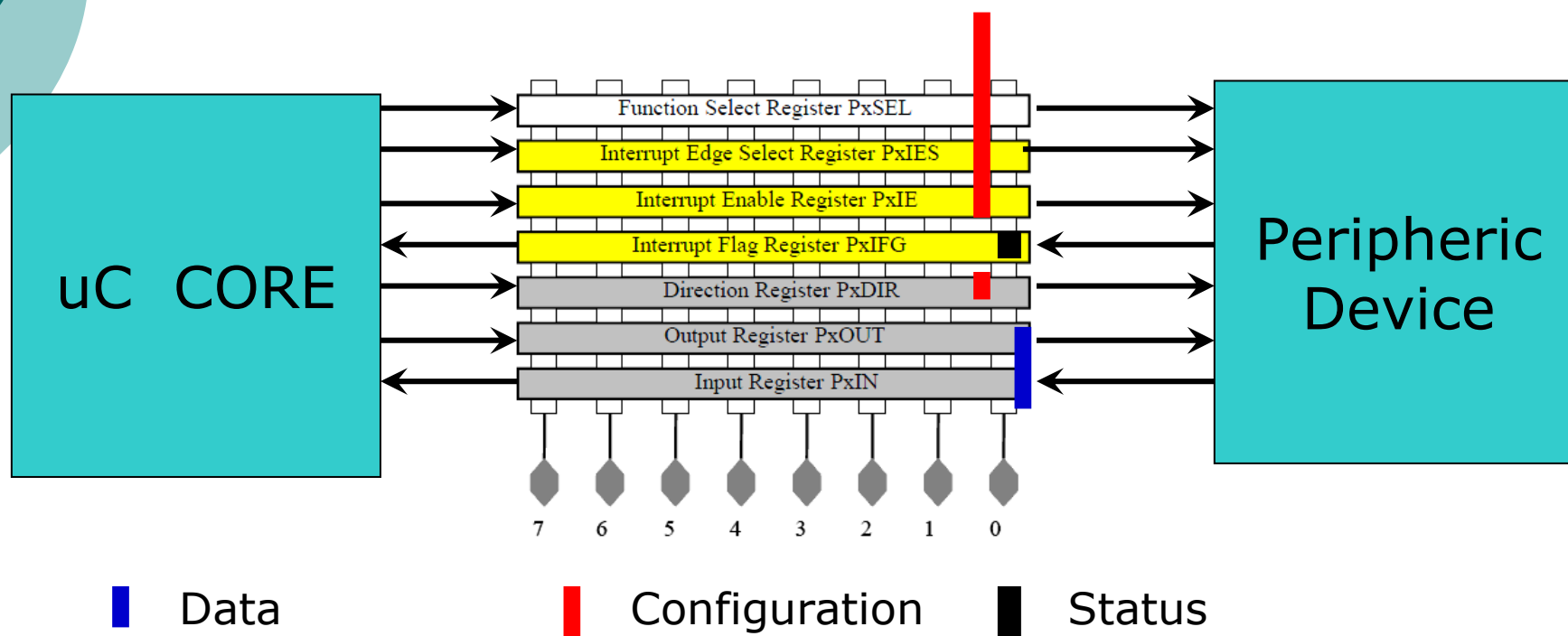


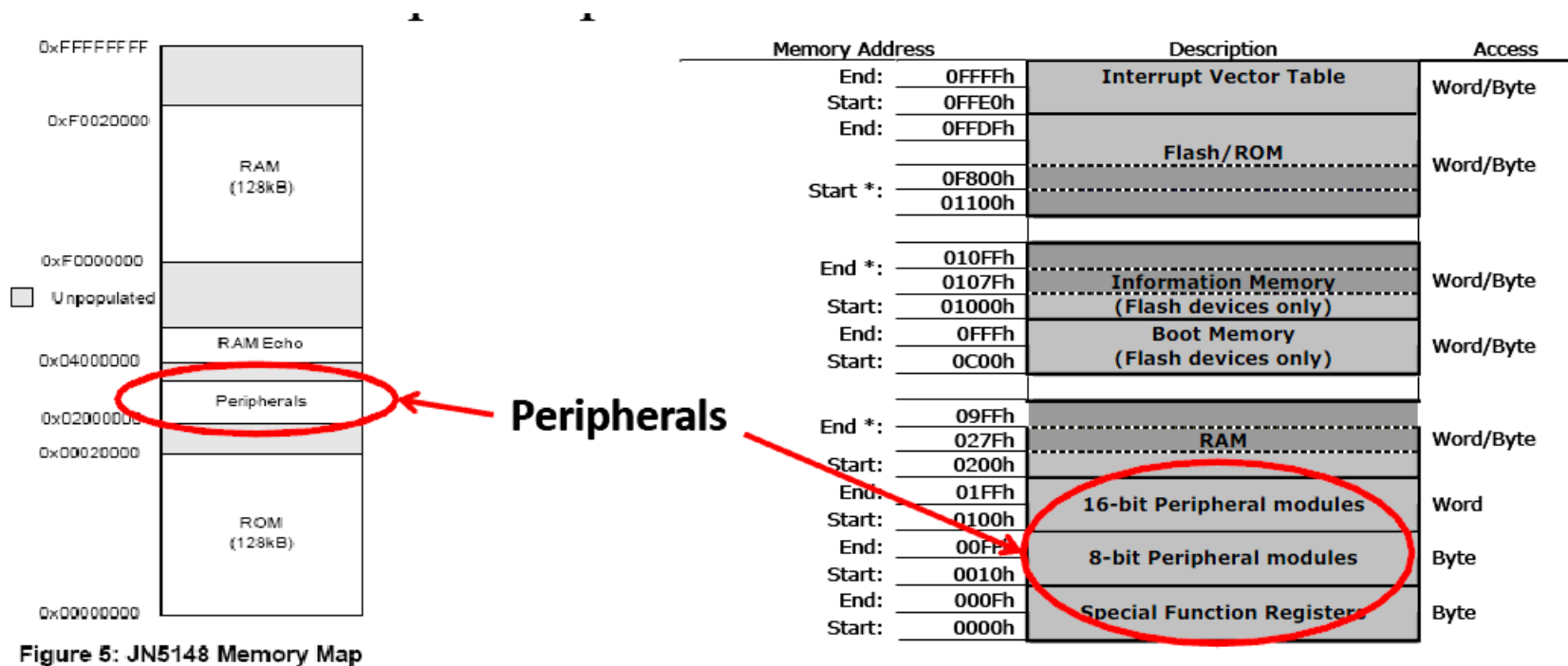
Figure 5: JN5148 Memory Map

Microcontrollori – Periferiche Interne

Peripherals registers

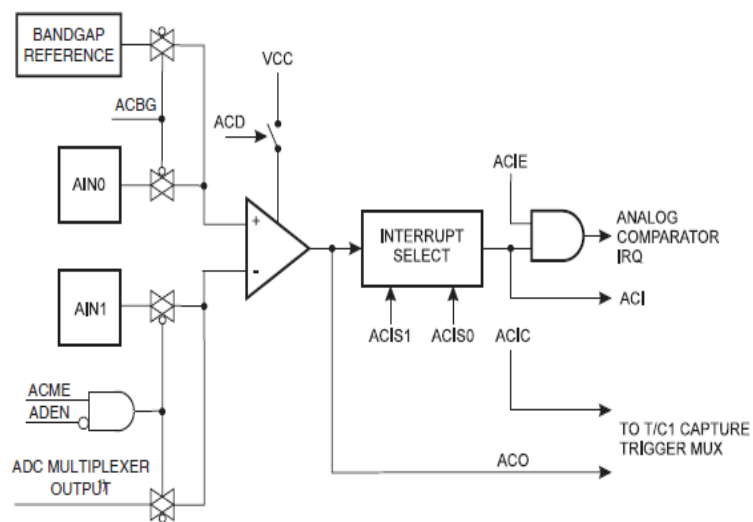


Microcontrollori – Periferiche Interne



Microcontrollori – Analogical Device

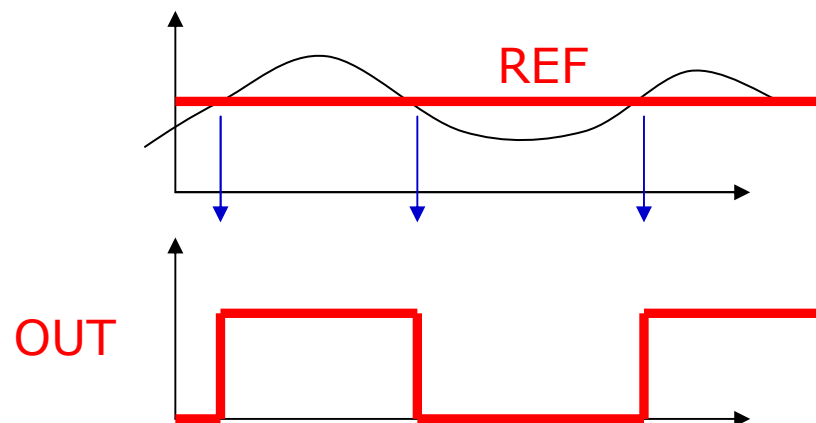
Comparator



- Monitoring of external analog signals.

- Internally reference voltage generator

- Externally reference voltage applicable



Microcontrollori – Analogical Device

ADC

Risoluzione

Indica il numero di bit di uscita:

10, 12, 16, 24 Bit ADC

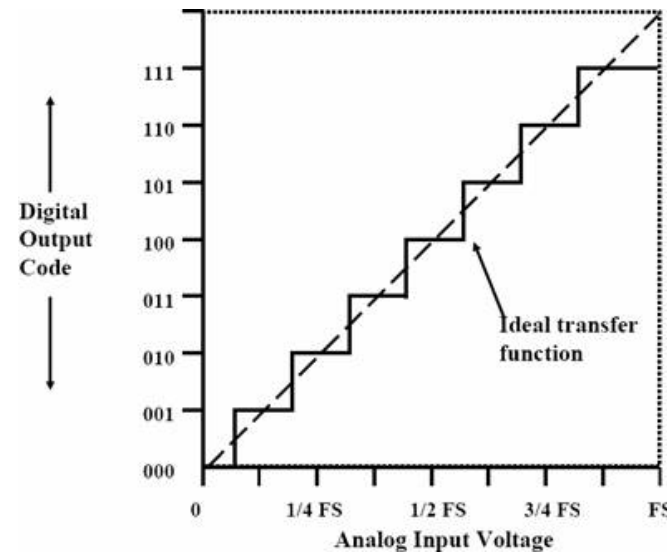
La variazione minima che si riesce a discriminare è legata alla risoluzione

Accuratezza

Livello di conformità fra dato convertito e dato analogico

Velocità di conversione

Massimo data rate espresso in sample per second (sps)



$$V_{LSB} = \frac{V_{ref}}{2^n}$$

LSB= Least Significant Bit

Microcontrollori – Analogical Device

ADC

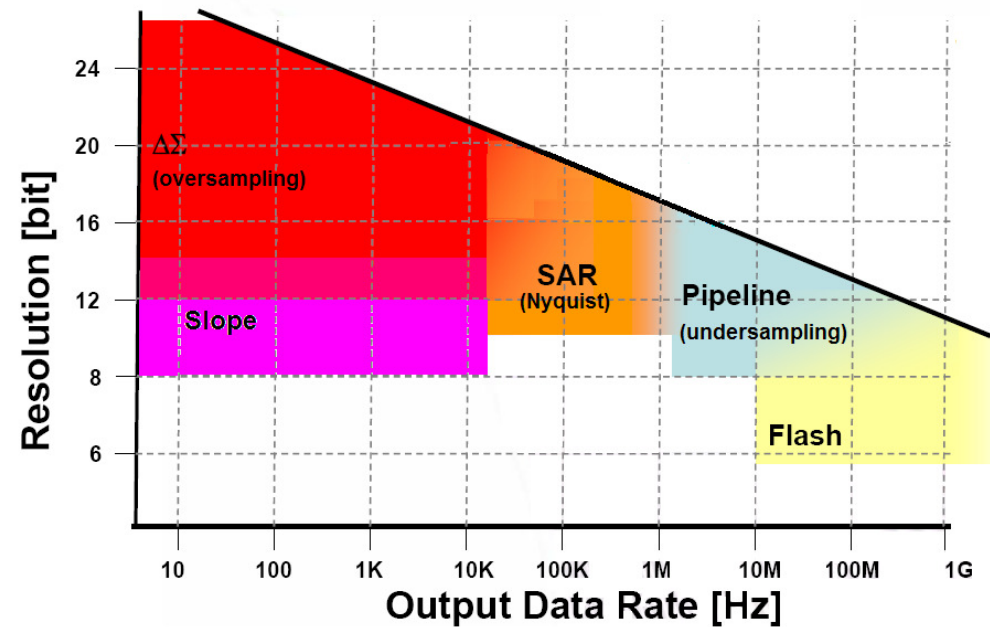
Successive Approximation (SAR)

Sigma Delta (SD or $\Delta\Sigma$)

Slope or Dual Slope

Pipeline

Flash





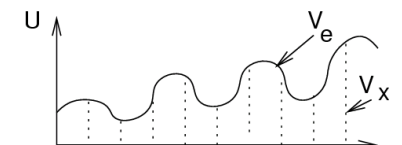
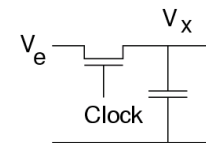
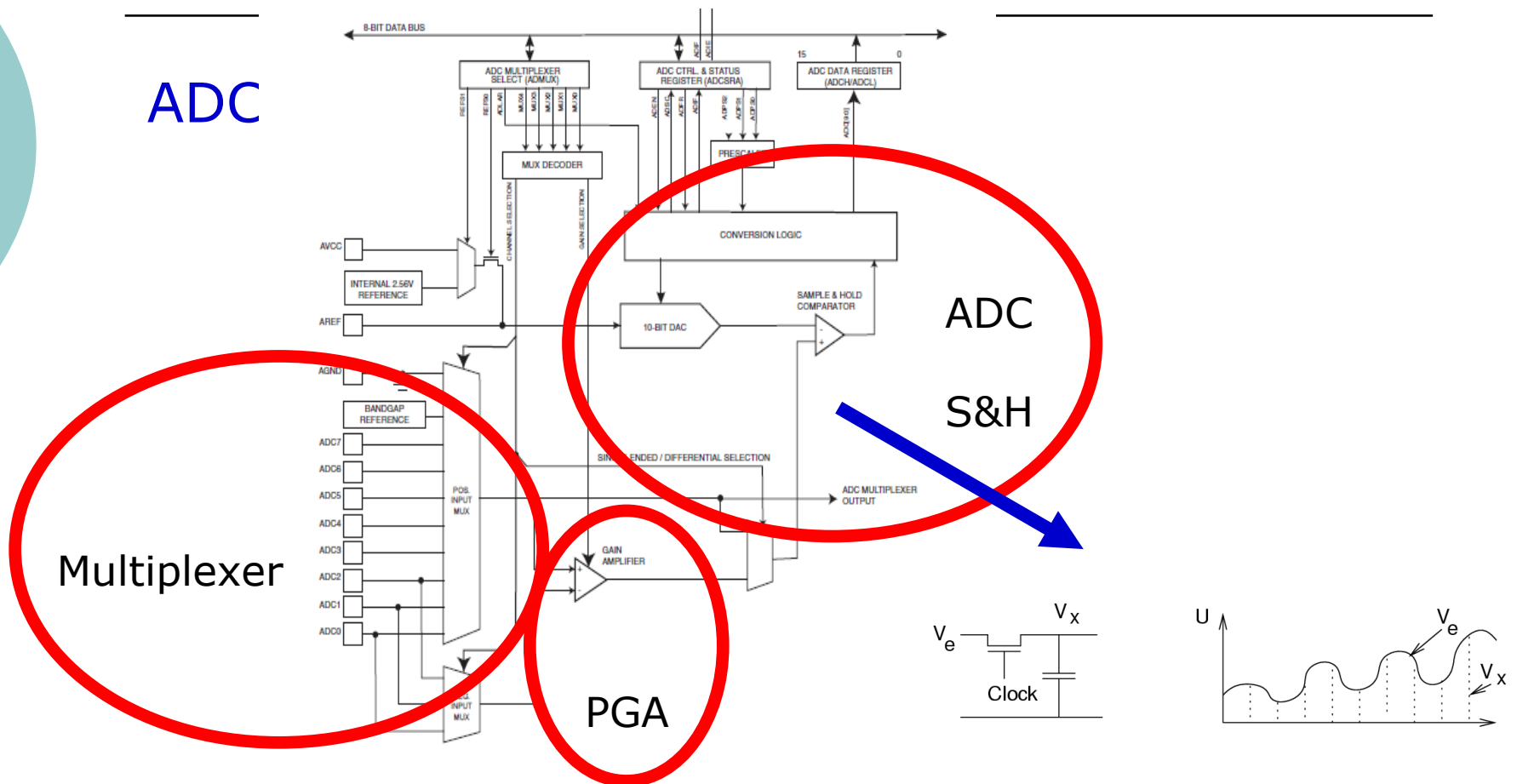
Microcontrollori – Analogical Device

ADC

ADC architecture	Resolution	Conversion rate	Advantages	Disadvantages
SAR	≤ 18 bit	< 5 Msps	Zero-cycle latency Low latency-time High accuracy Low power Simple operation High resolution	Sample rates 2-5 MHz
SD	≤ 24 bit $\leq 16-18$ bit	< 625 ksps < 10 Msps	High stability Low power Moderate cost	Cycle-latency Low speed
Pipeline	≤ 16 bit	< 500 Msps	Higher speeds Higher bandwidth	Lower resolution Delay/Data latency Power requirements

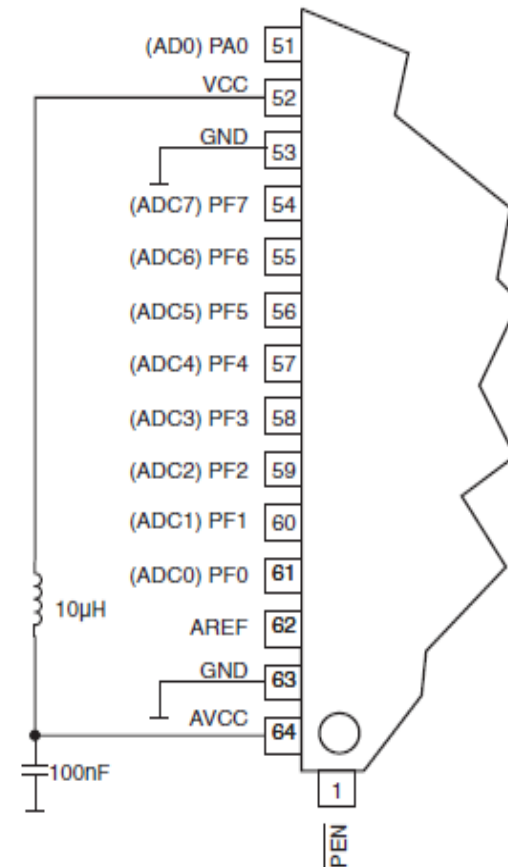
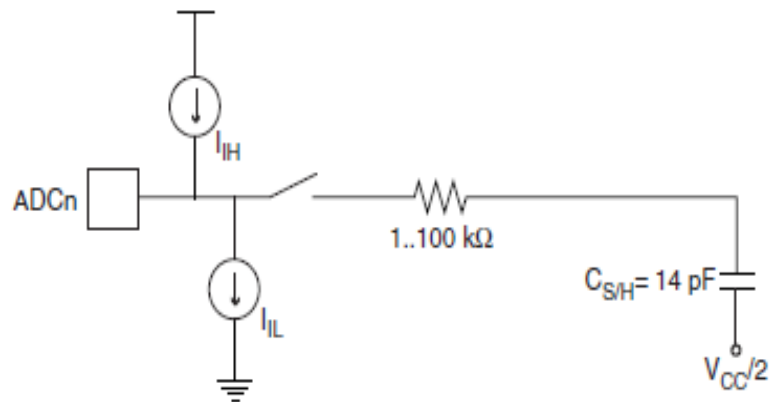
Microcontrollori – Analogical Device

ADC



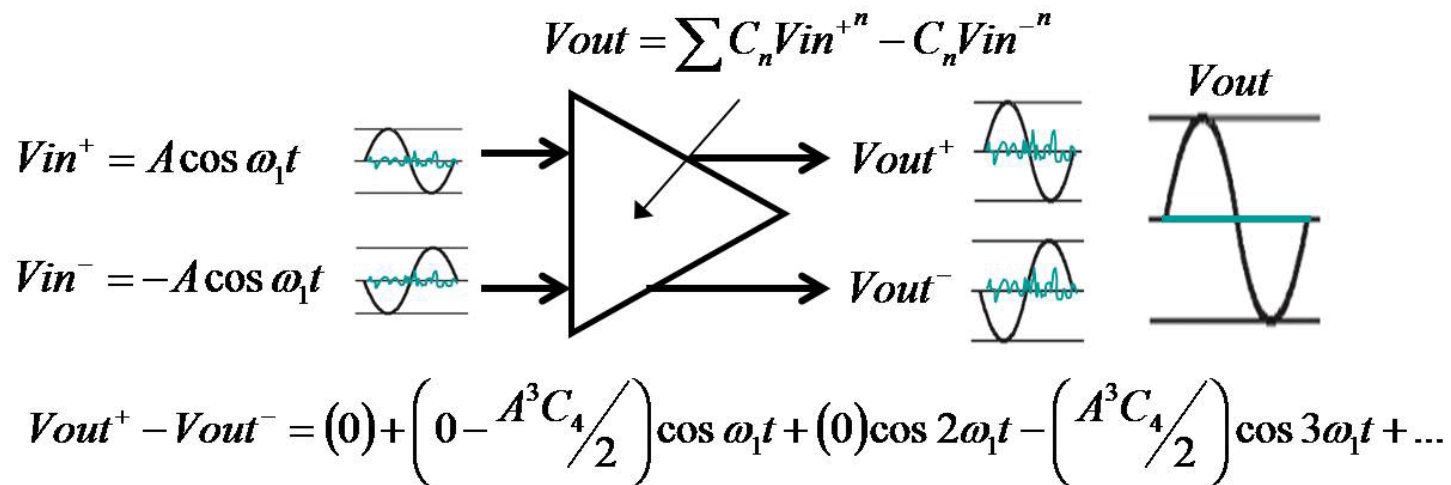
Microcontrollori – Analogical Device

ADC – Single Ended Input



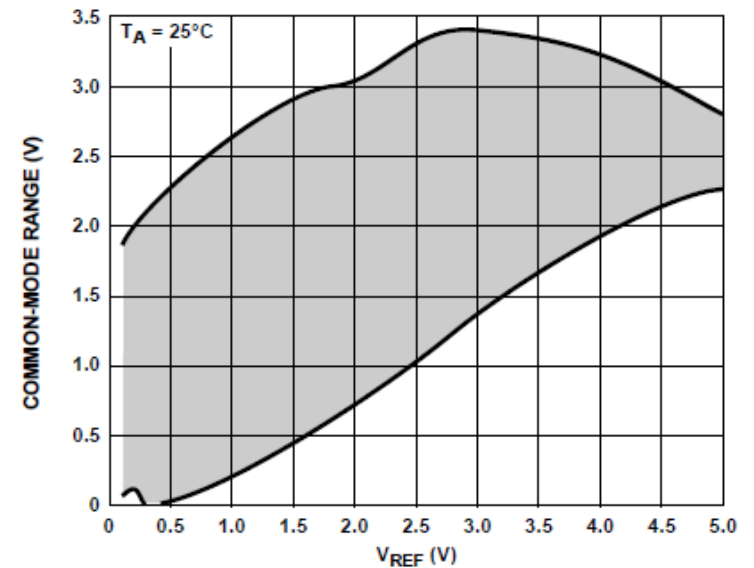
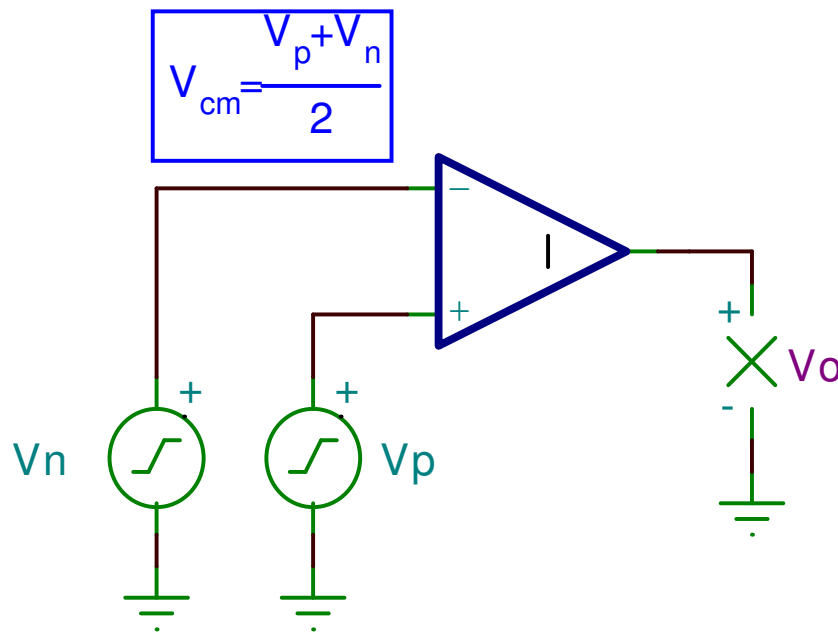
Microcontrollori – Analogical Device

ADC – Differential Input



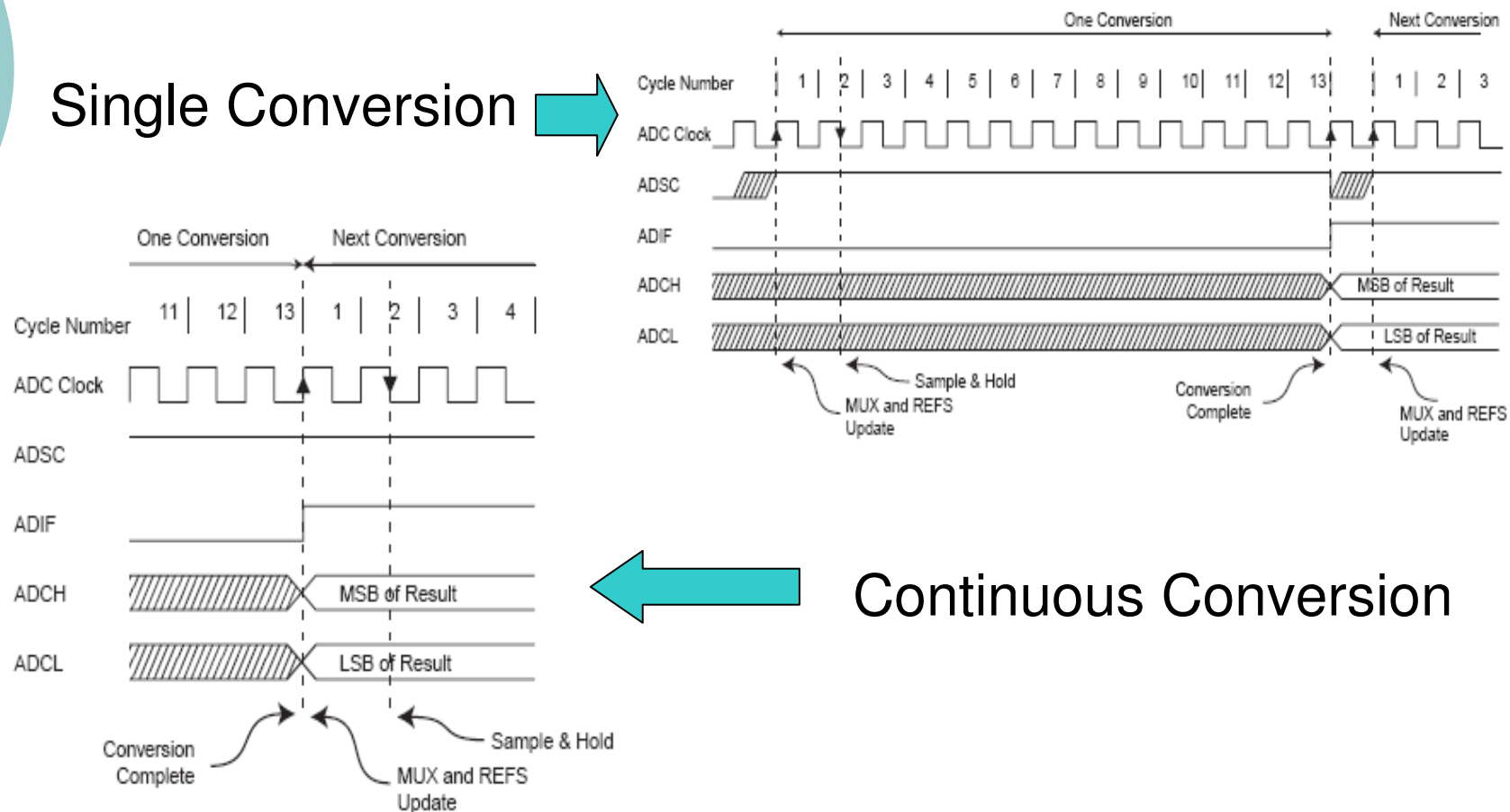
Microcontrollori – Analogical Device

ADC – Differential Input



Microcontrollori – Analogical Device

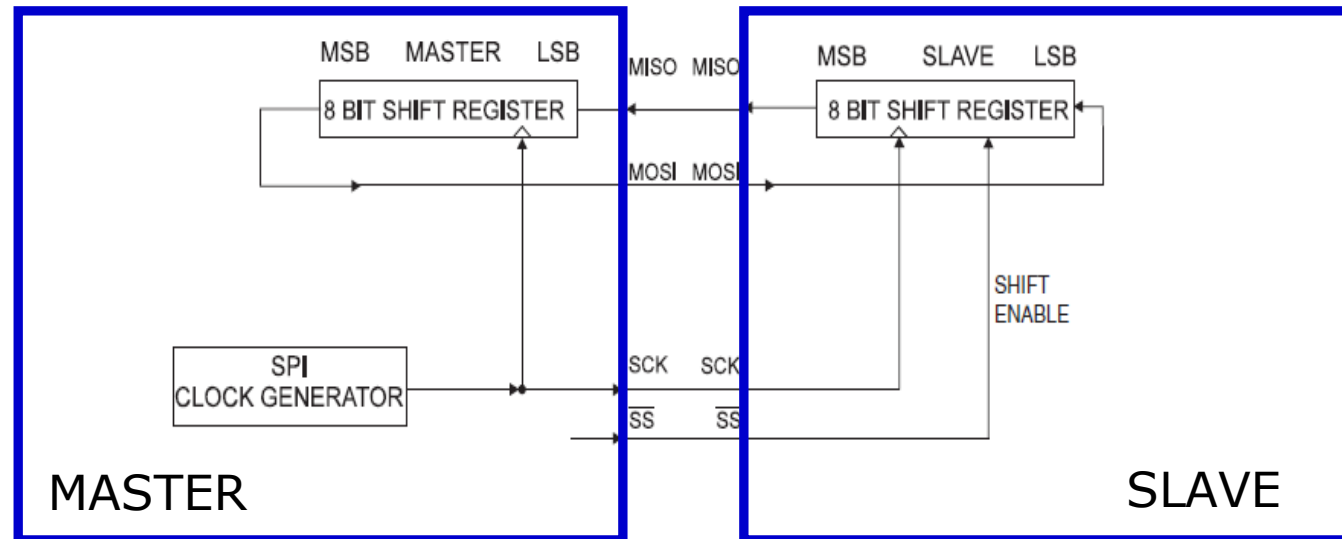
Single Conversion



Continuous Conversion

Microcontrollori – Comm. Interface

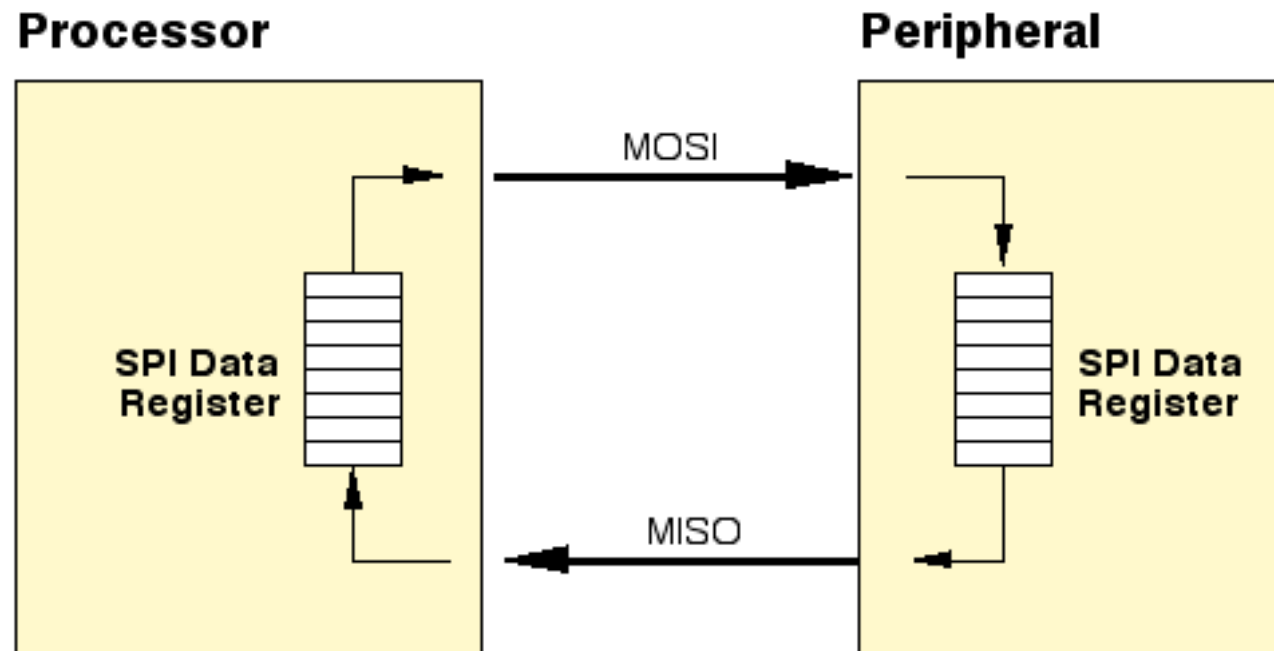
SPI



Pin	Direction, Master SPI	Direction, Slave SPI
MOSI	User Defined	Input
MISO	Input	User Defined
SCK	User Defined	Input
\overline{SS}	User Defined	Input

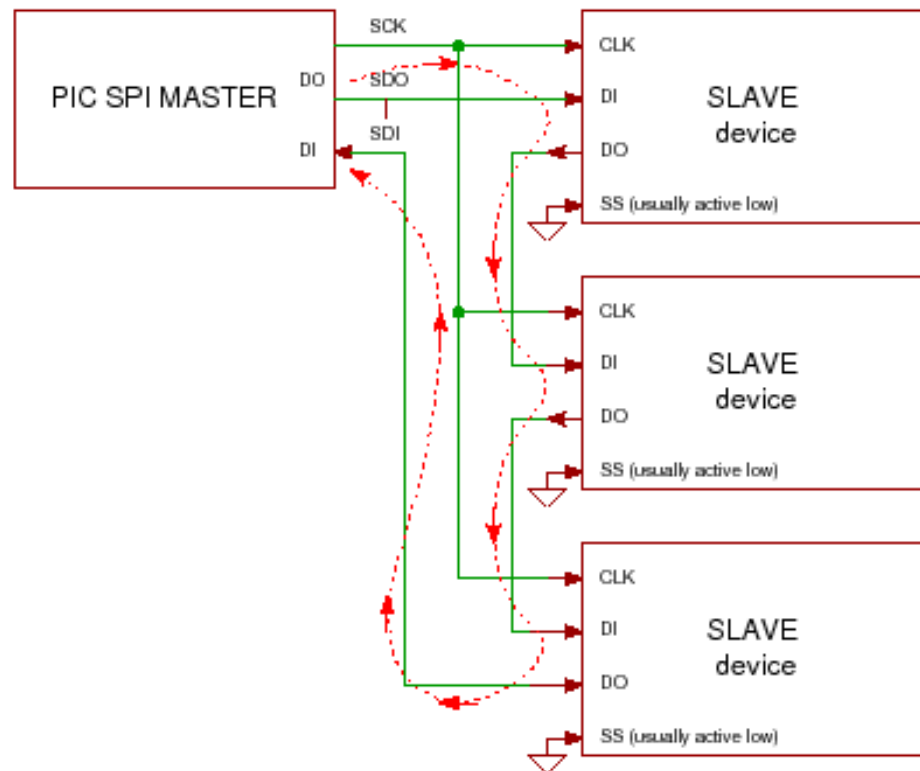
Microcontrollori – Comm. Interface

SPI



Microcontrollori – Comm. Interface

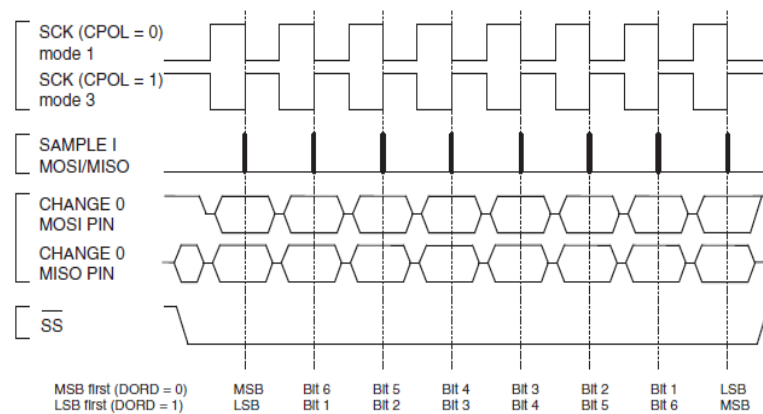
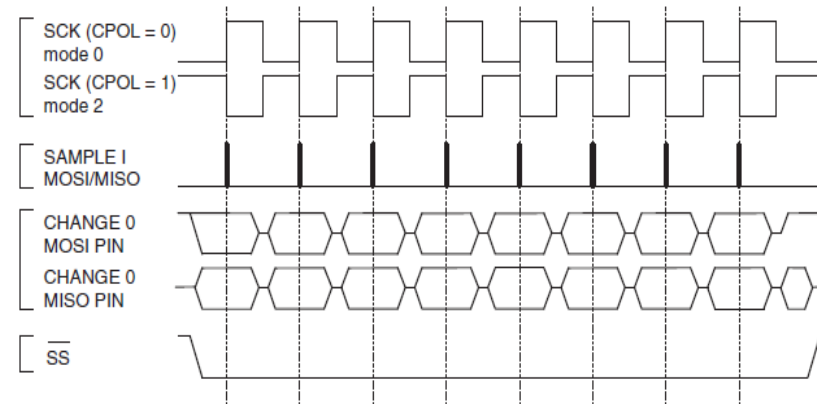
SPI



Microcontrollori – Comm. Interface

SPI

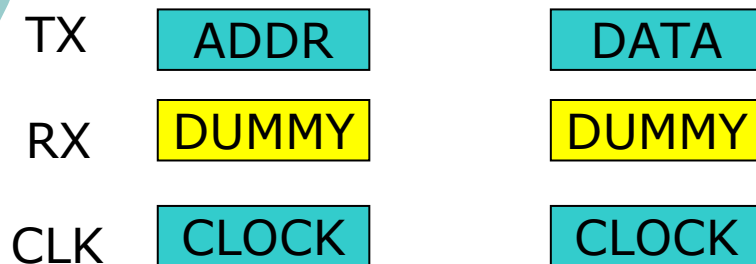
POLARITY!!!!!!



Microcontrollori – Comm. Interface

SPI Code

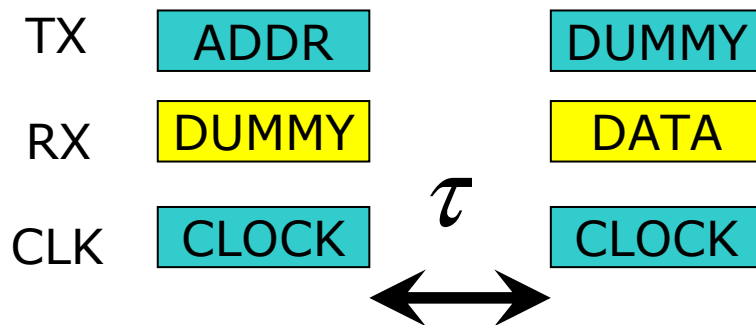
WRITE



```

// Configuration for SPI
packet.chip = TARGET_ADDRESS;
packet.addr[0] = 27; //(VIRTUALMEM_ADDR >> 16) & 0xff;
packet.addr_length = TARGET_ADDR_LGT;
writel_data[0]=0x18; //scala 500
// Where to find the data to be written
packet.buffer = (void *) writel_data;
// How many bytes do we want to write
packet.length = PATTERN_TEST_LENGTH;
//print_dbg ("Writing data 27\r\n");
// Write data to TARGET
status = twi_master_write (TWIM, &packet);
// Check status of transfer
    
```

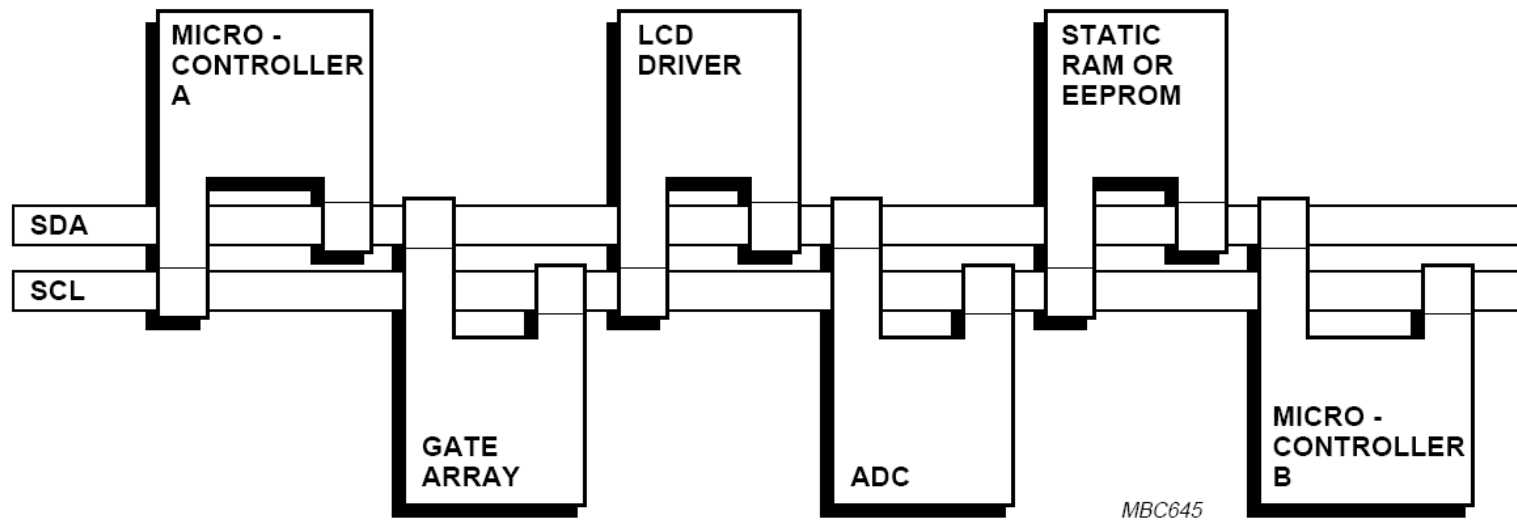
READ



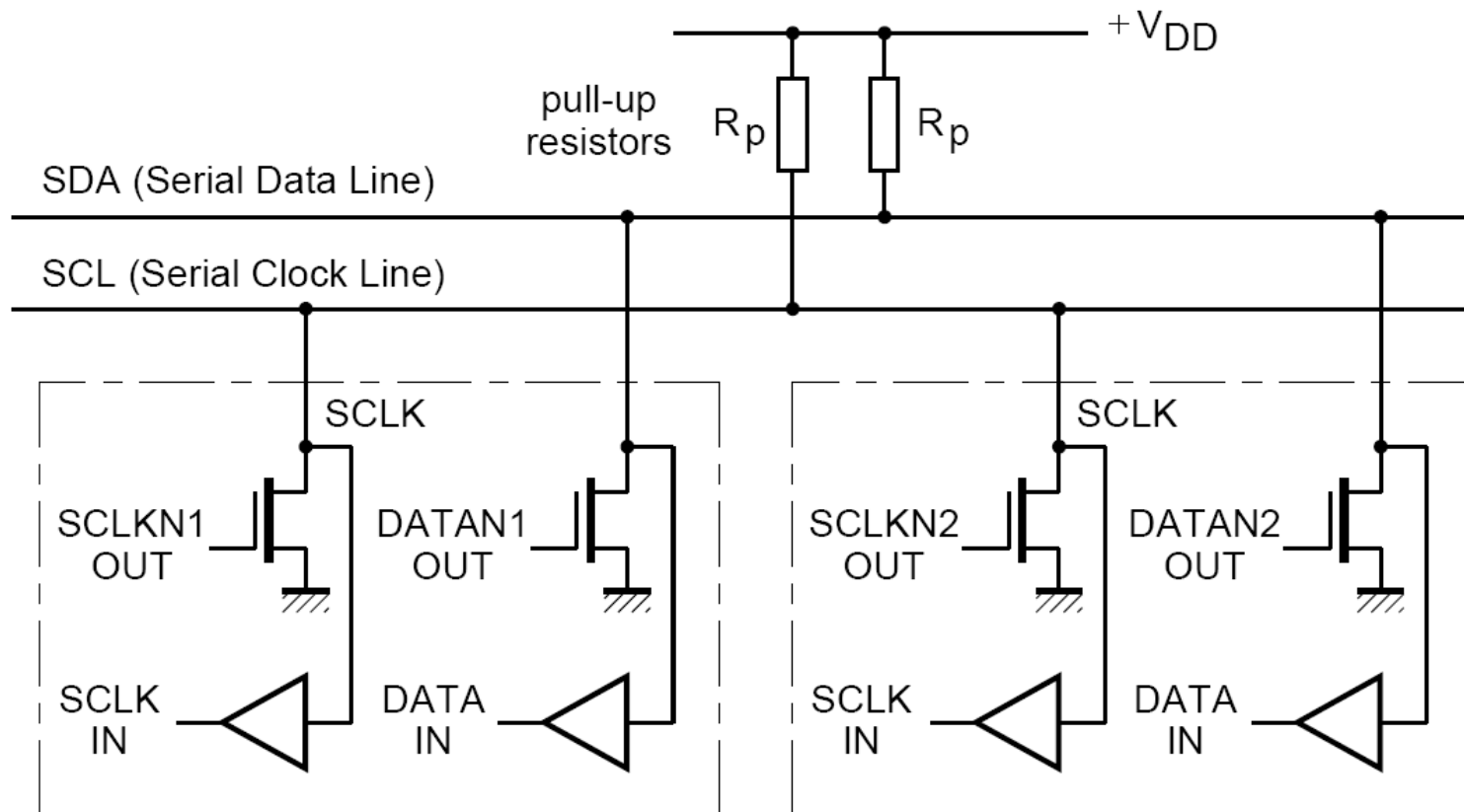
```

// Configuration for SPI
packet_received.chip = TARGET_ADDRESS;
packet_received.addr_length = TARGET_ADDR_LGT;
packet_received.length = 6; //PATTERN_TEST_LENGTH;
packet_received.addr[0] = 59; //(VIRTUALMEM_ADDR >> 16) & 0xff;
packet_received.buffer = readl_data;
status = twi_master_read (TWIM, &packet_received);
// Check status of transfer
    
```

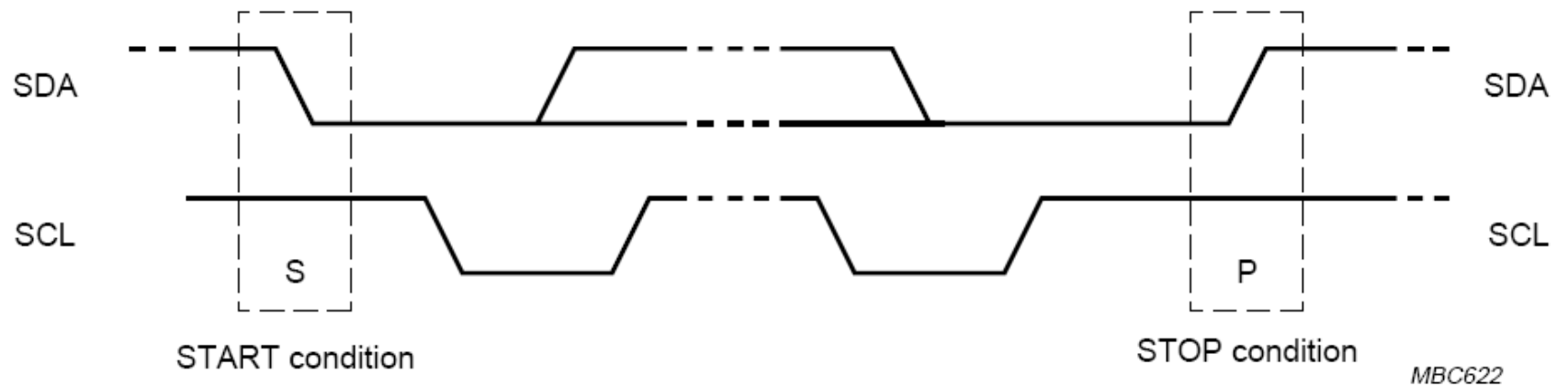
I2C



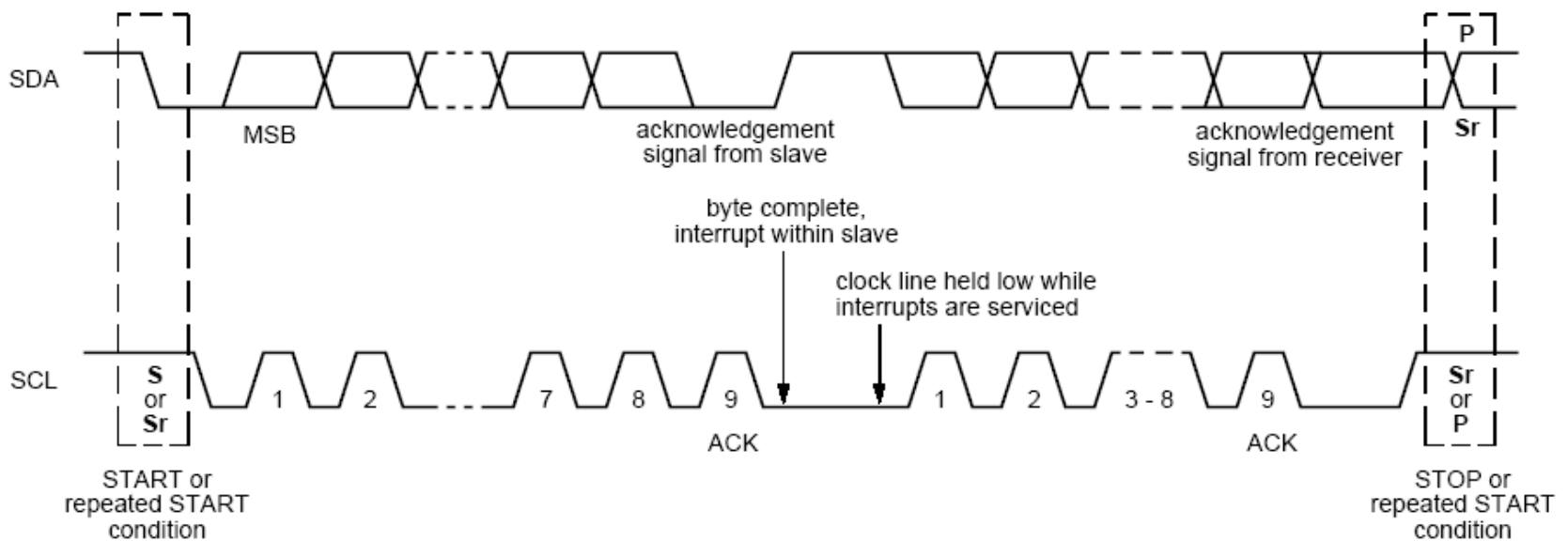
I2C



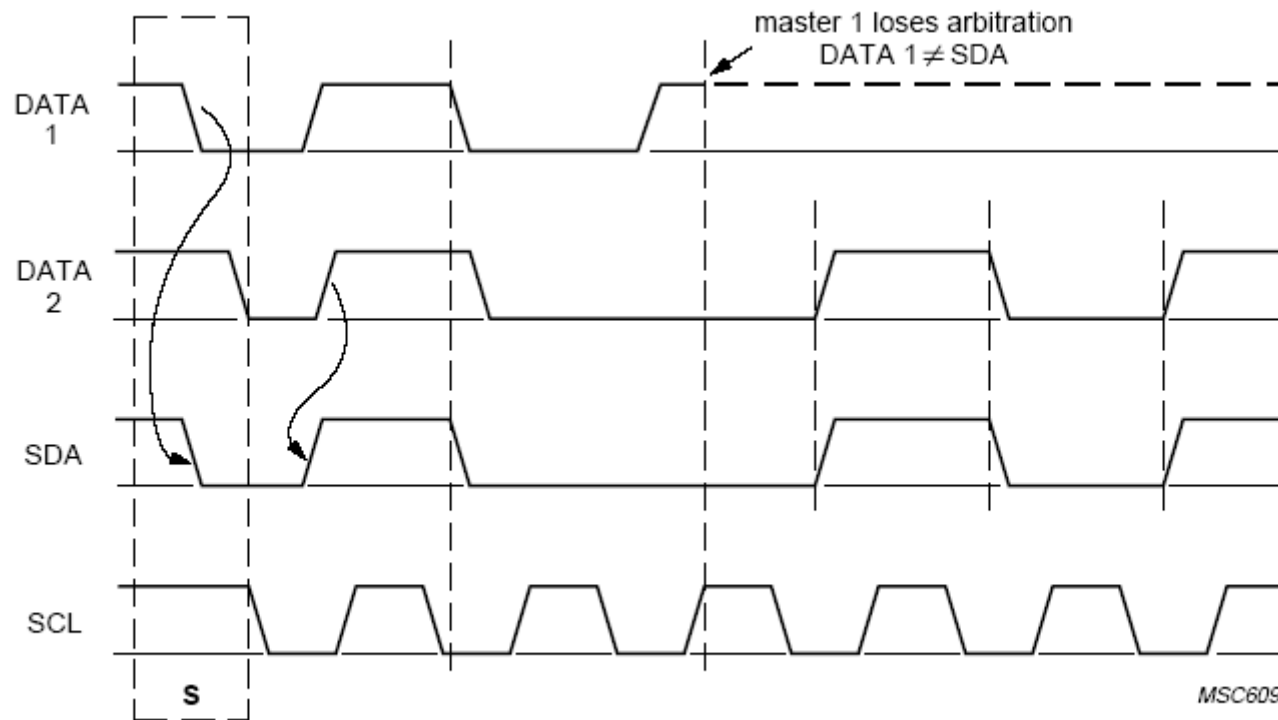
I2C Start Stop



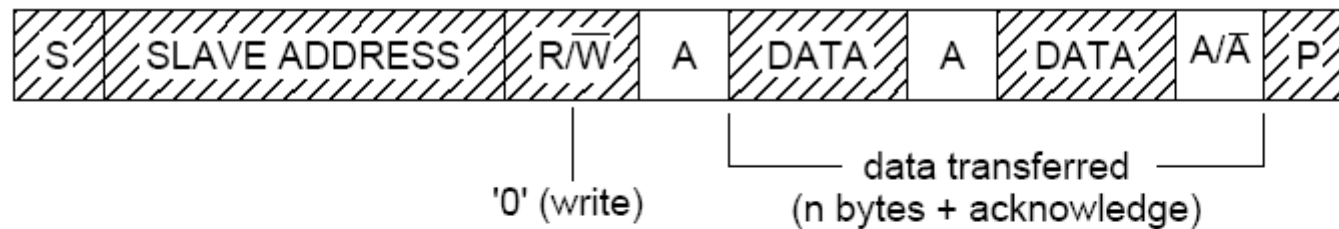
I2C Data Transfer





I2C Arbitration



I2C Trasmissione



 from master to slave

 from slave to master

MBC605

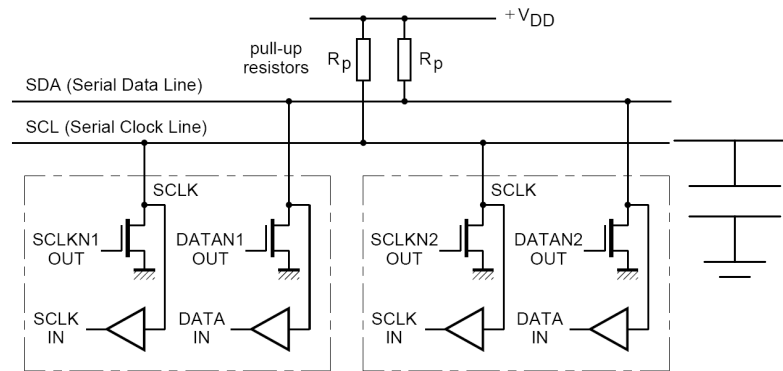
A = acknowledge (SDA LOW)

\bar{A} = not acknowledge (SDA HIGH)

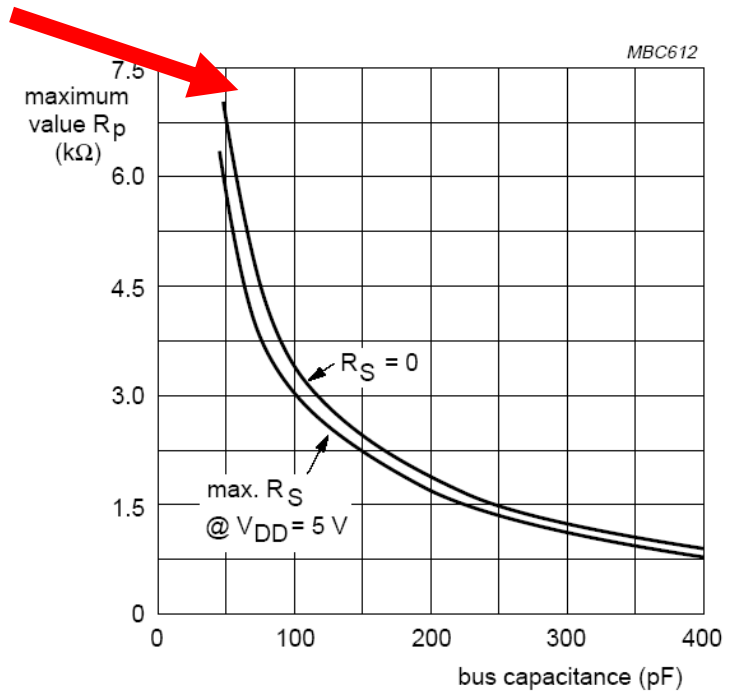
S = START condition

P = STOP condition

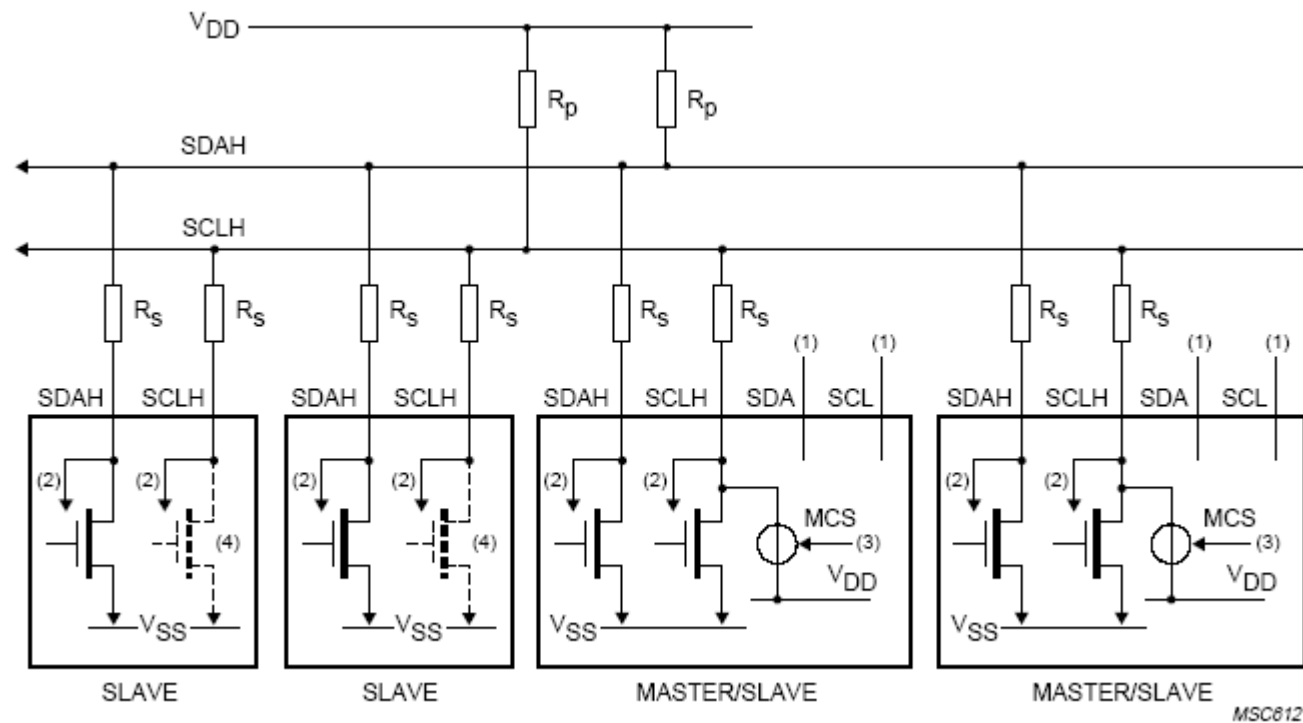
I2C Rp e C



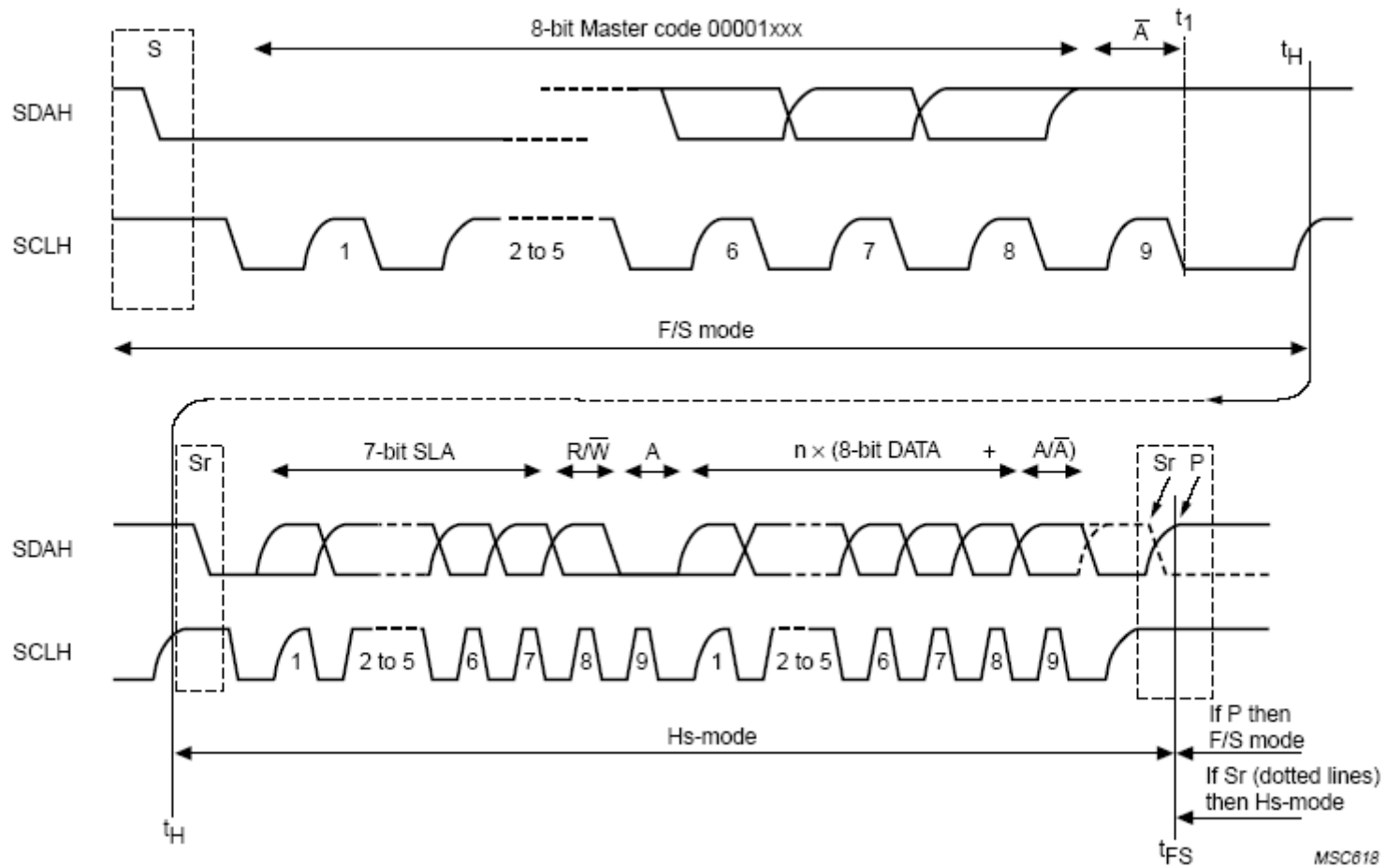
$$C_L \propto (L; D)$$



I2C HS mode



I2C HS Mode



I2C Velocità di comunicazione

TRANSFER BETWEEN	SERIAL BUS SYSTEM CONFIGURATION			
	Hs + FAST + STANDARD	Hs + FAST	Hs + STANDARD	FAST + STANDARD
Hs <--> Hs	0 to 3.4 Mbit/s	0 to 3.4 Mbit/s	0 to 3.4 Mbit/s	–
Hs <--> Fast	0 to 100 kbit/s	0 to 400 kbit/s	–	–
Hs <--> Standard	0 to 100 kbit/s	–	0 to 100 kbit/s	–
Fast <--> Standard	0 to 100 kbit/s	–	–	0 to 100 kbit/s
Fast <--> Fast	0 to 100 kbit/s	0 to 400 kbit/s	–	0 to 100 kbit/s
Standard <--> Standard	0 to 100 kbit/s	–	0 to 100 kbit/s	0 to 100 kbit/s