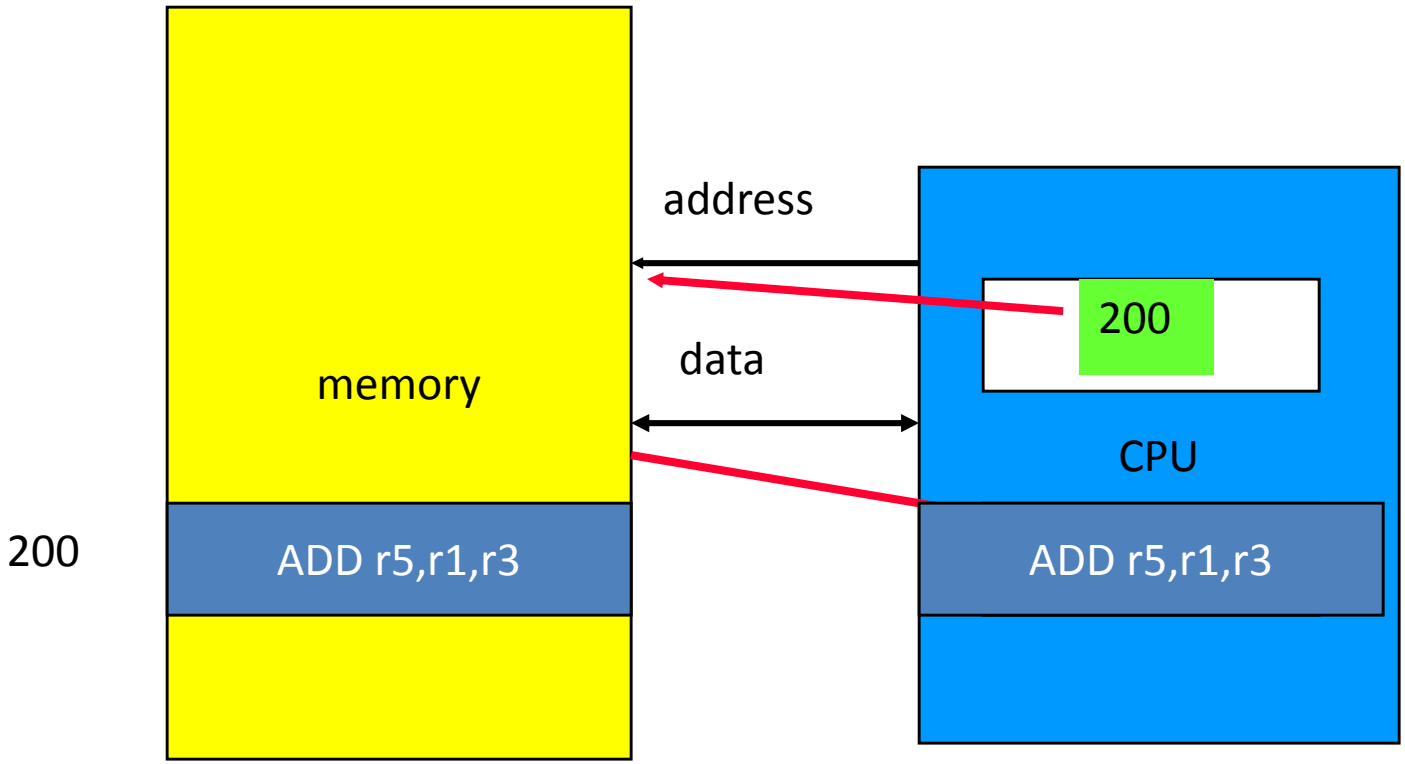
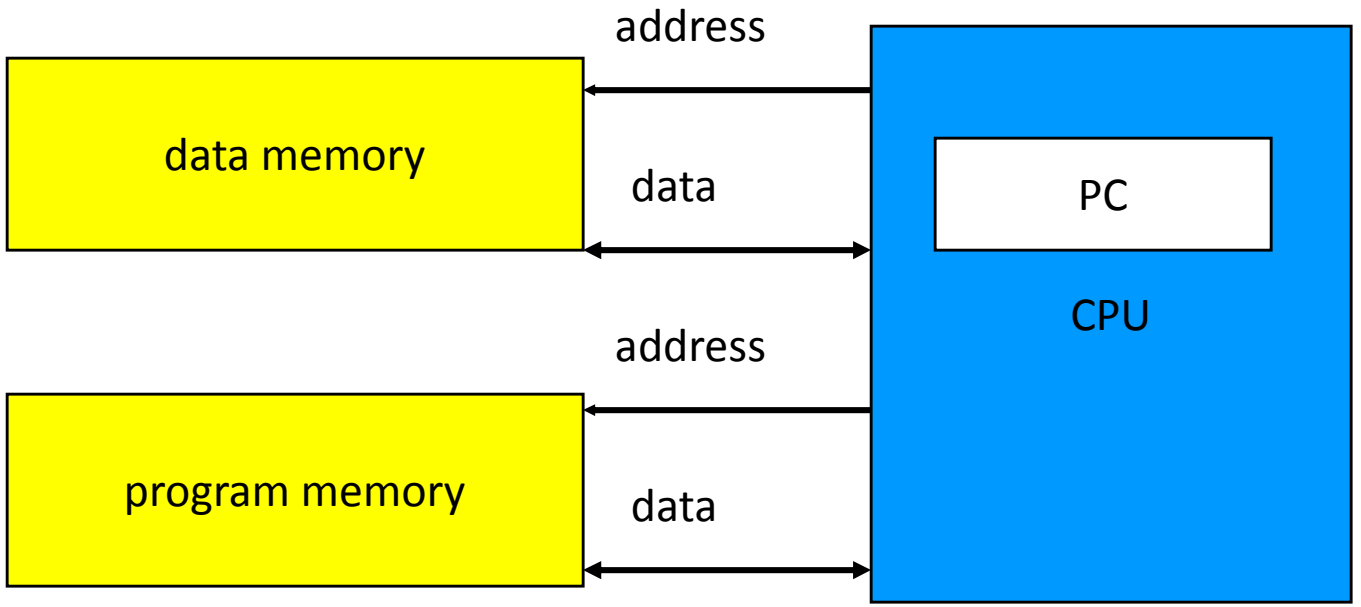
CPU + memory



Harvard architecture



RISC vs. CISC

- Complex instruction set computer (CISC):
  - many addressing modes;
  - many operations.
- Reduced instruction set computer (RISC):
  - load/store;
  - pipelinable instructions.

Instruction set characteristics

- Fixed vs. variable length.
- Addressing modes.
- Number of operands.
- Types of operands.

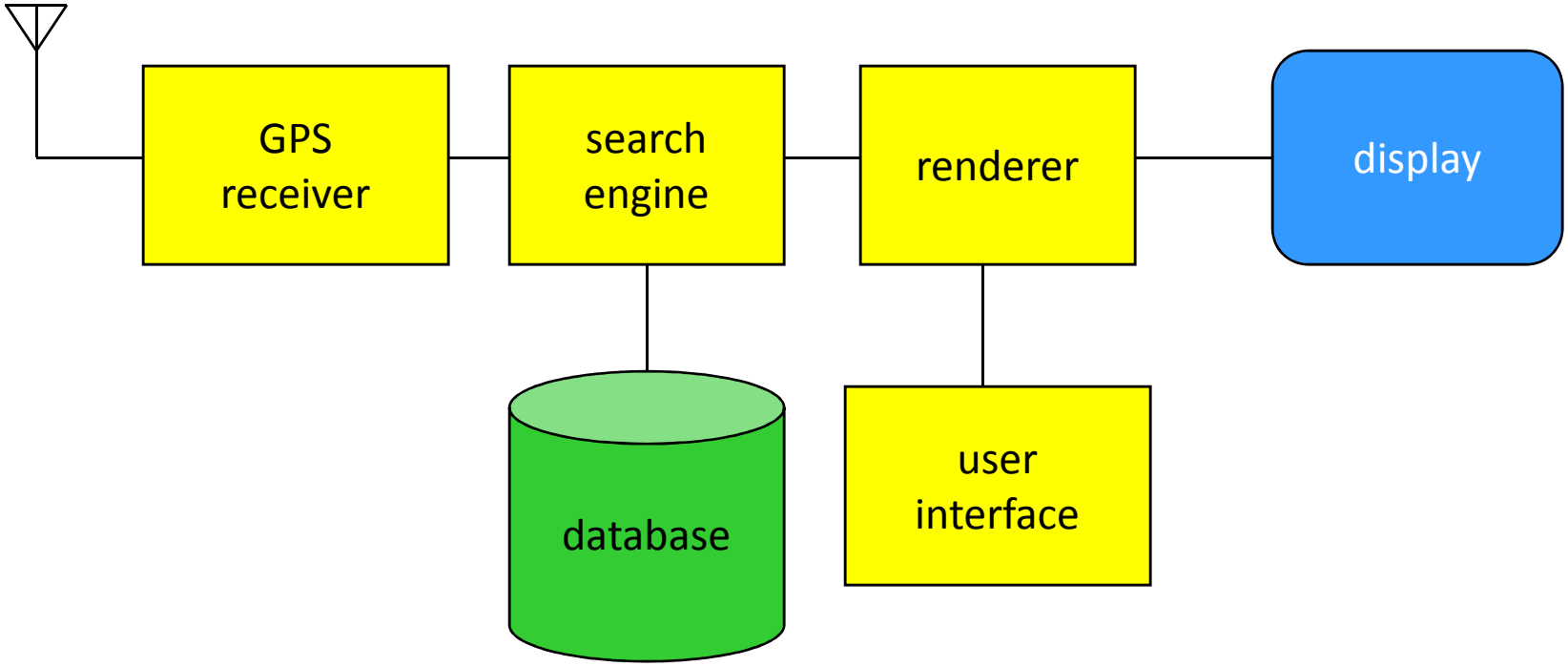
Programming model

- Programming model: registers visible to the programmer.
- Some registers are not visible (IR).

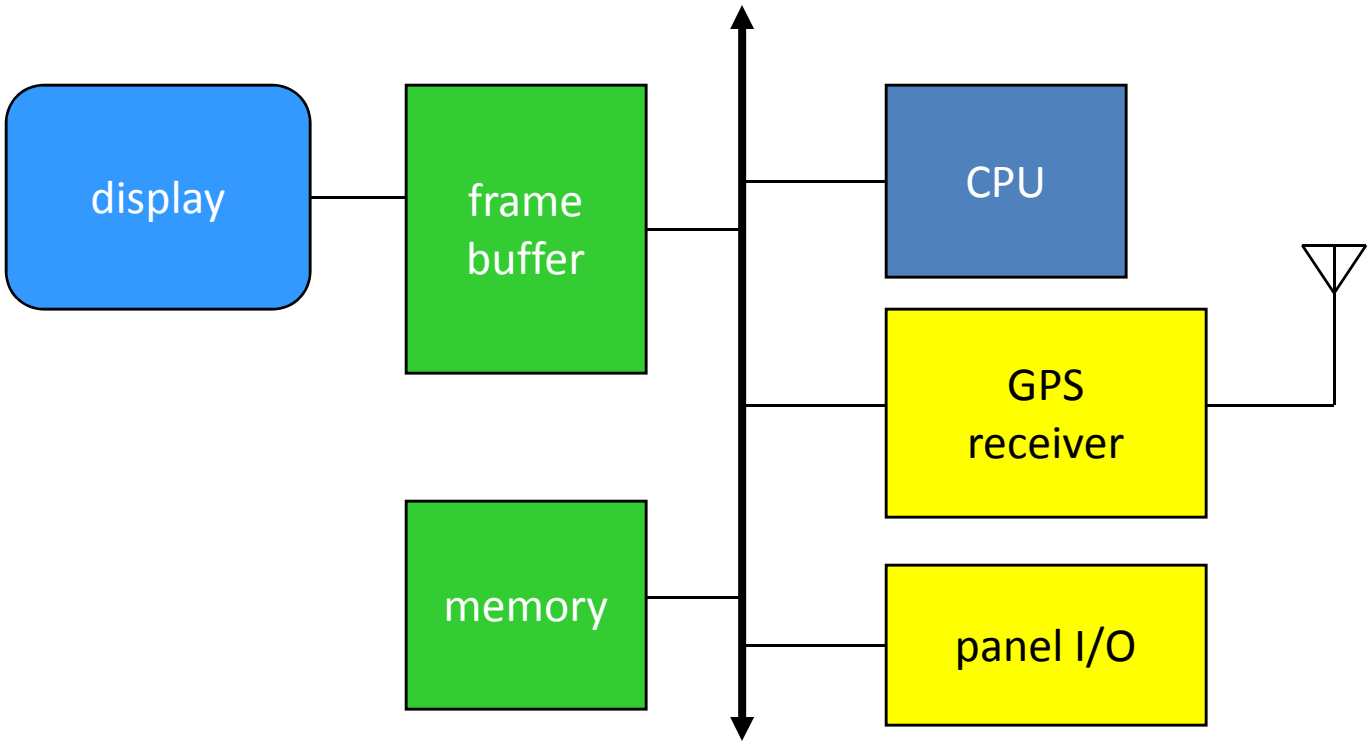
Multiple implementations

- Successful architectures have several implementations:
  - varying clock speeds;
  - different bus widths;
  - different cache sizes;
  - etc.

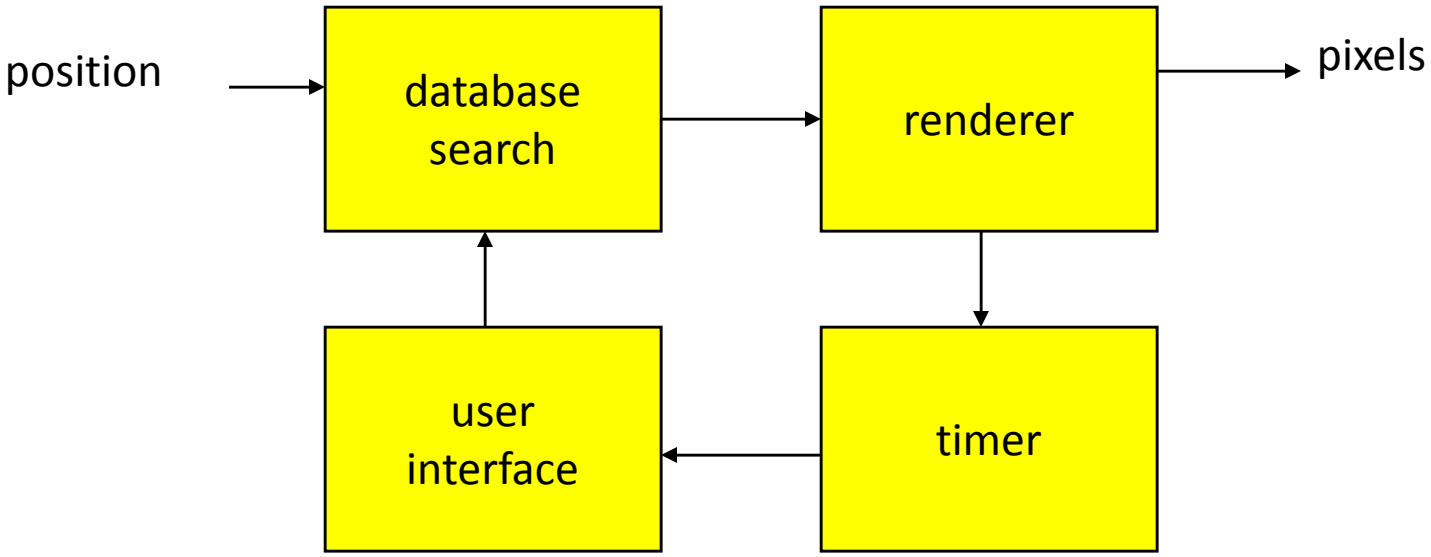
GPS moving map block diagram



GPS moving map hardware architecture

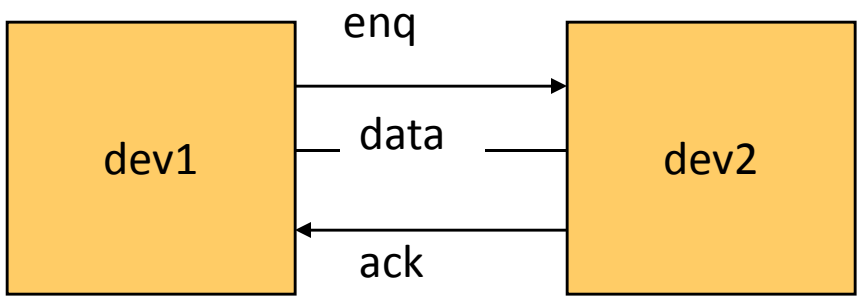


GPS moving map software architecture

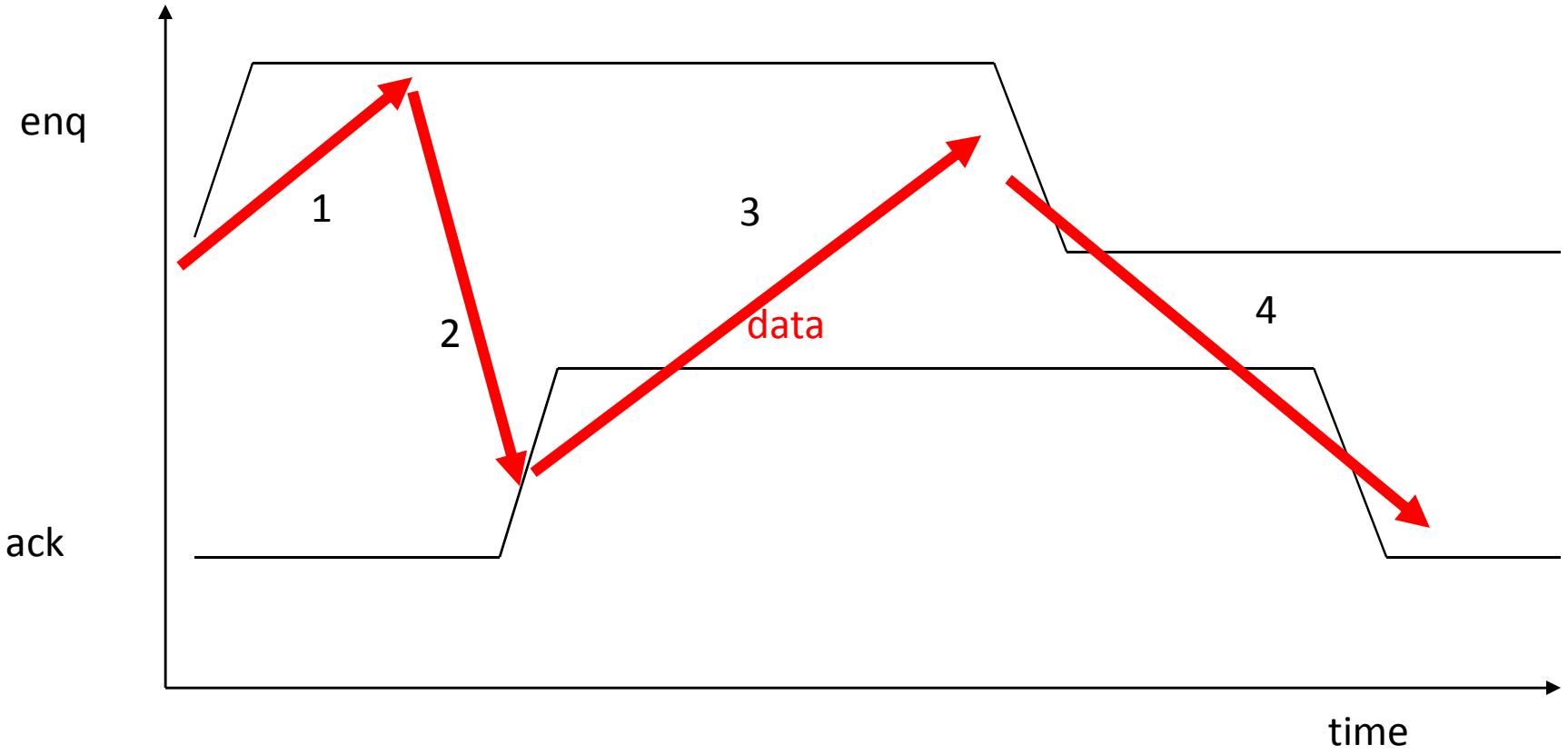


Four-cycle handshake

- Basis of many bus protocols.
- Uses two wires:
  - enq (enquiry);
  - ack (acknowledgment).



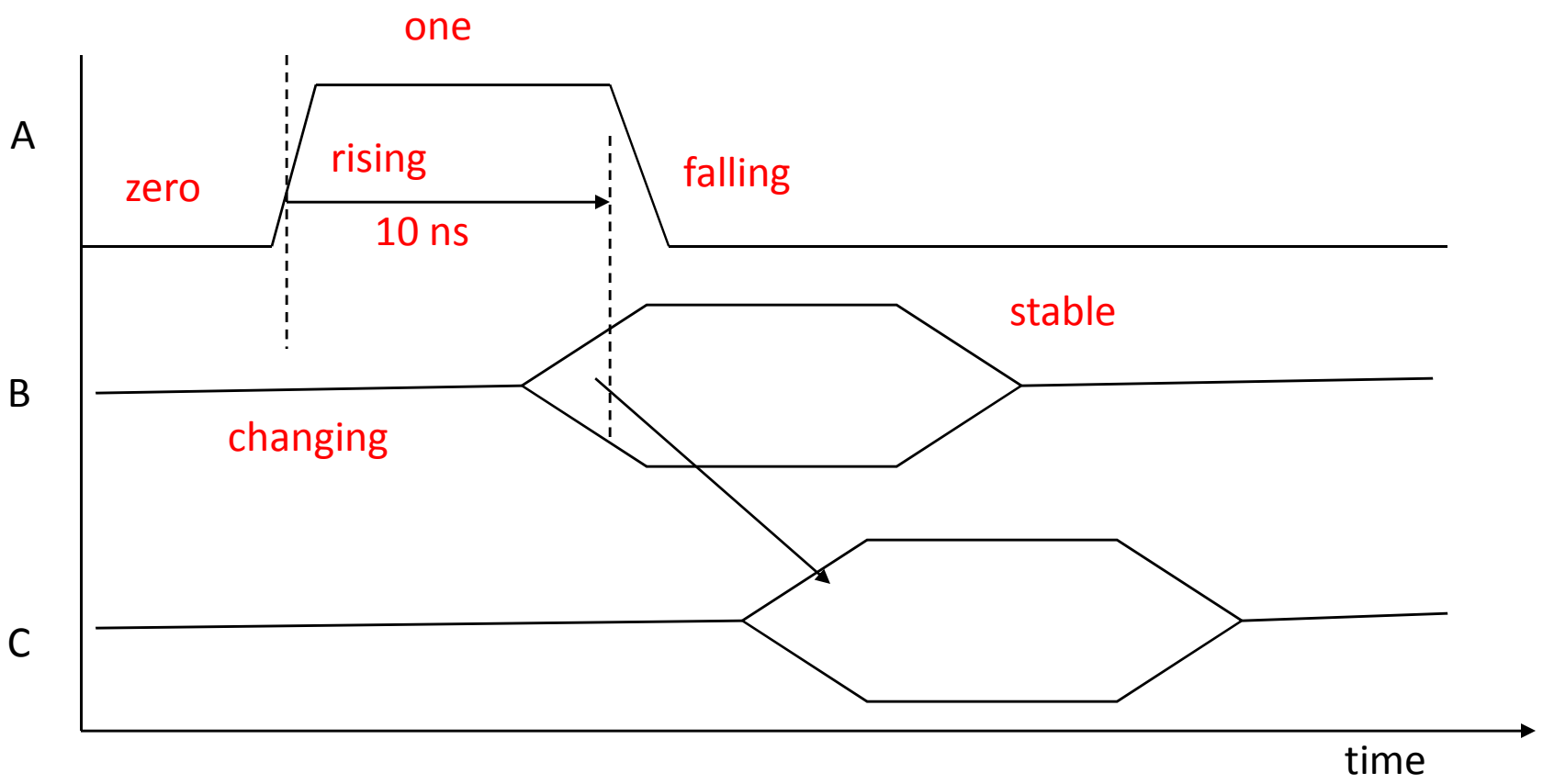
Four-cycle example



Typical bus signals

- Clock.
- R/W’: true when bus is reading.
- Address: a-bit bundle.
- Data: n-bit bundle.
- Data ready’.

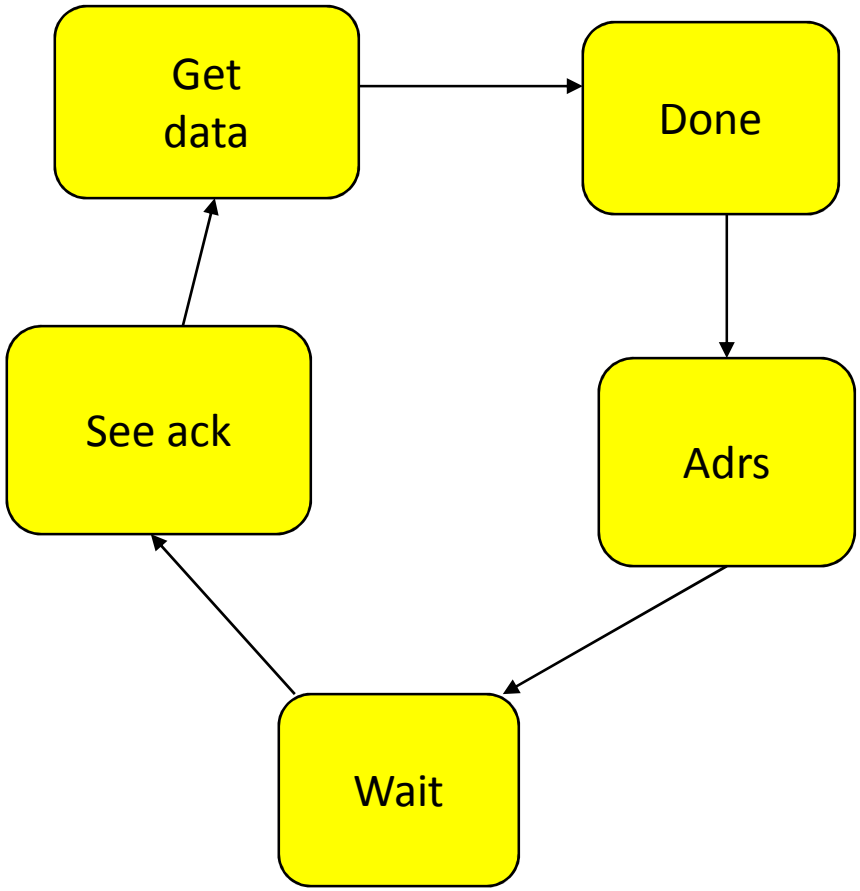
Timing diagrams



Typical bus timing for read

- CPU:
  - asserts address, address enable;
  - set R/W'=1.
- Memory:
  - asserts data;
  - asserts data ready'.
- CPU:
  - De-asserts address, address enable.

Bus read state diagram

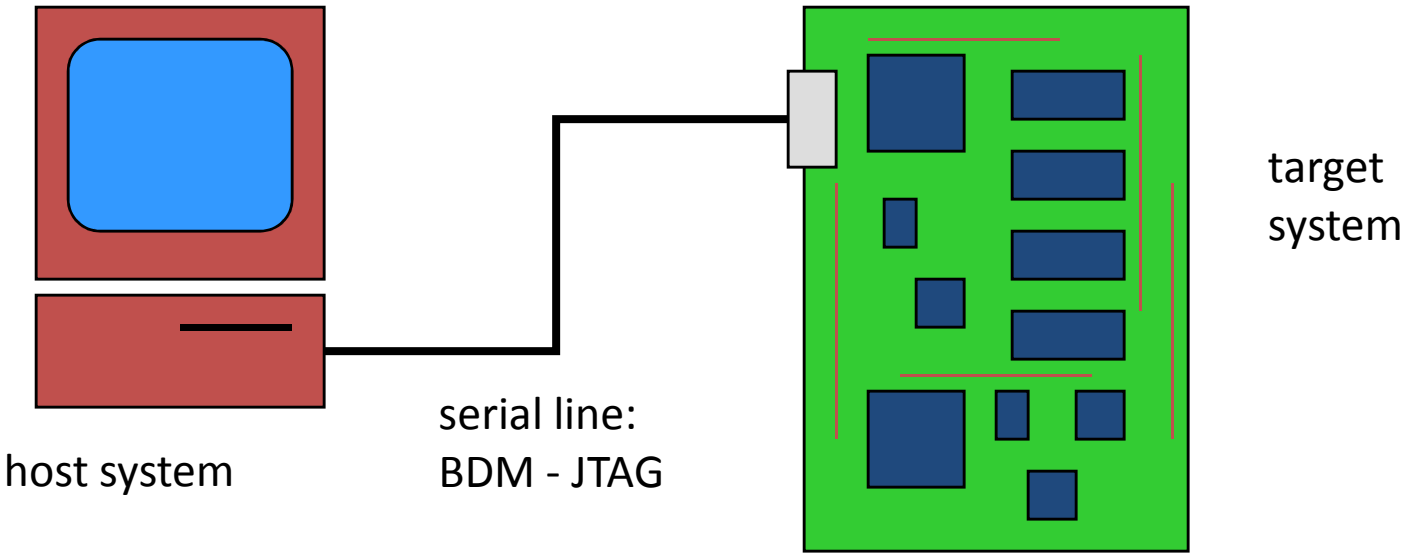


Transaction types

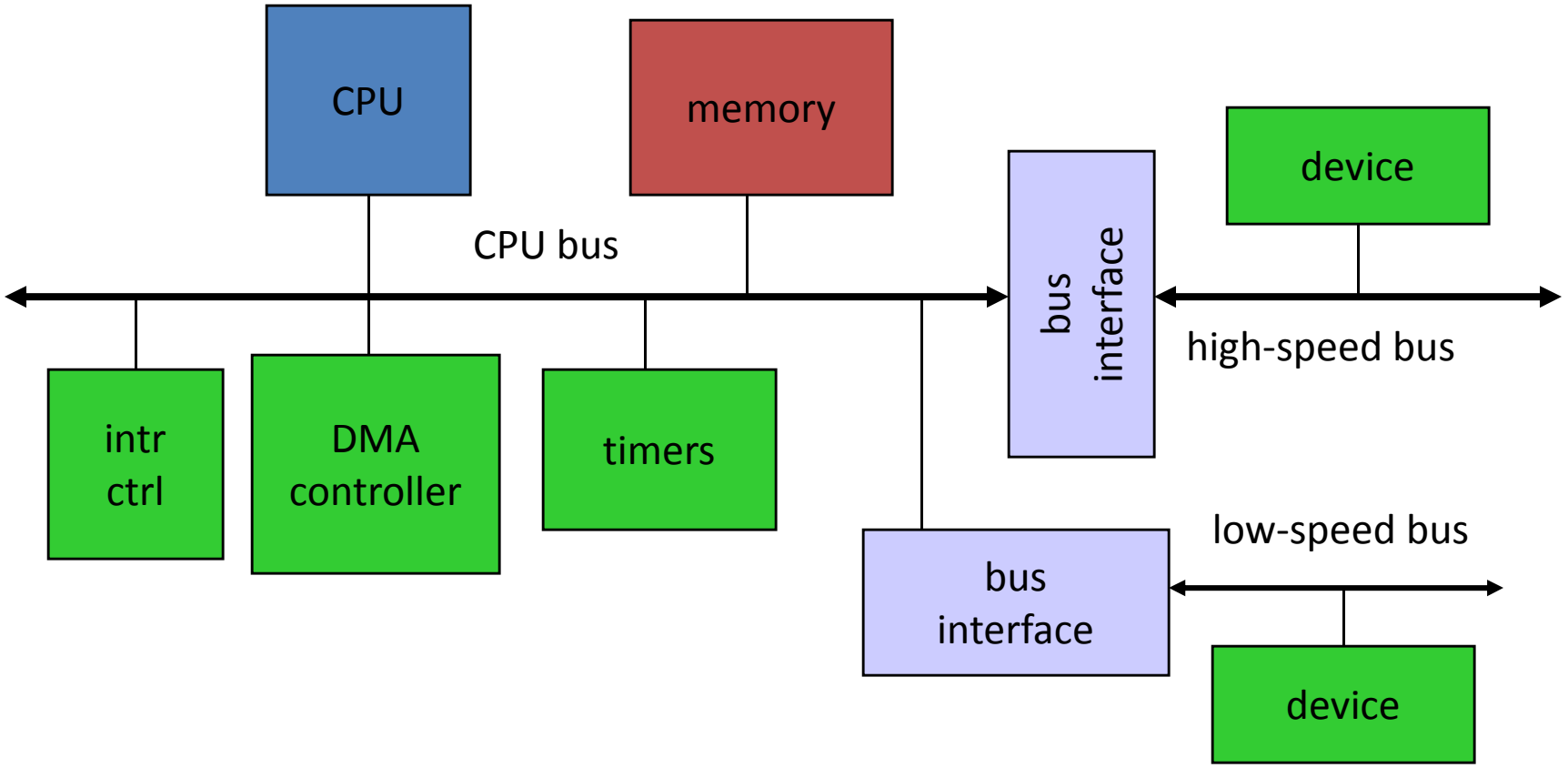
- Wait state:
  - state in a bus transaction to wait for acknowledgment.
- Disconnected transfer:
  - bus is freed during wait state.
- Burst:
  - multiple transfers.

Host/target design: Cross-Compilazione

- Use a host system to prepare software for target system:

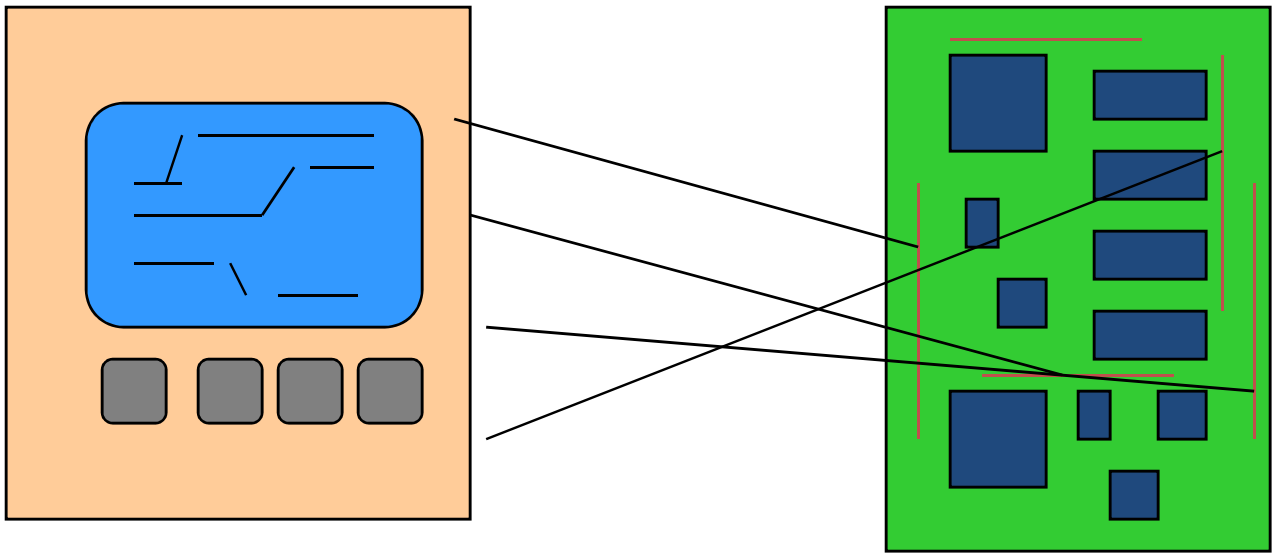


Typical PC hardware platform

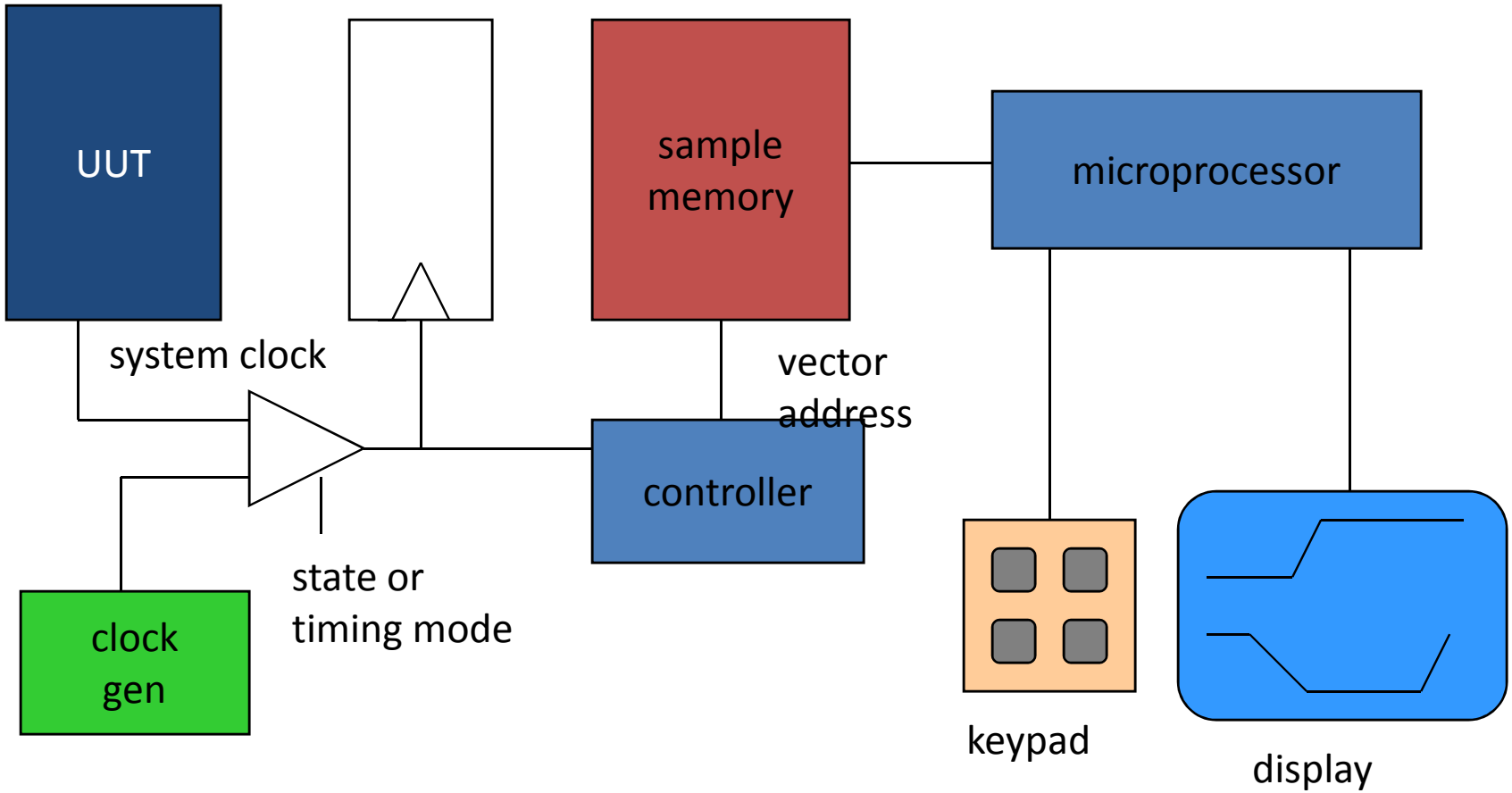


Logic analyzers

- A logic analyzer is an array of low-grade oscilloscopes:



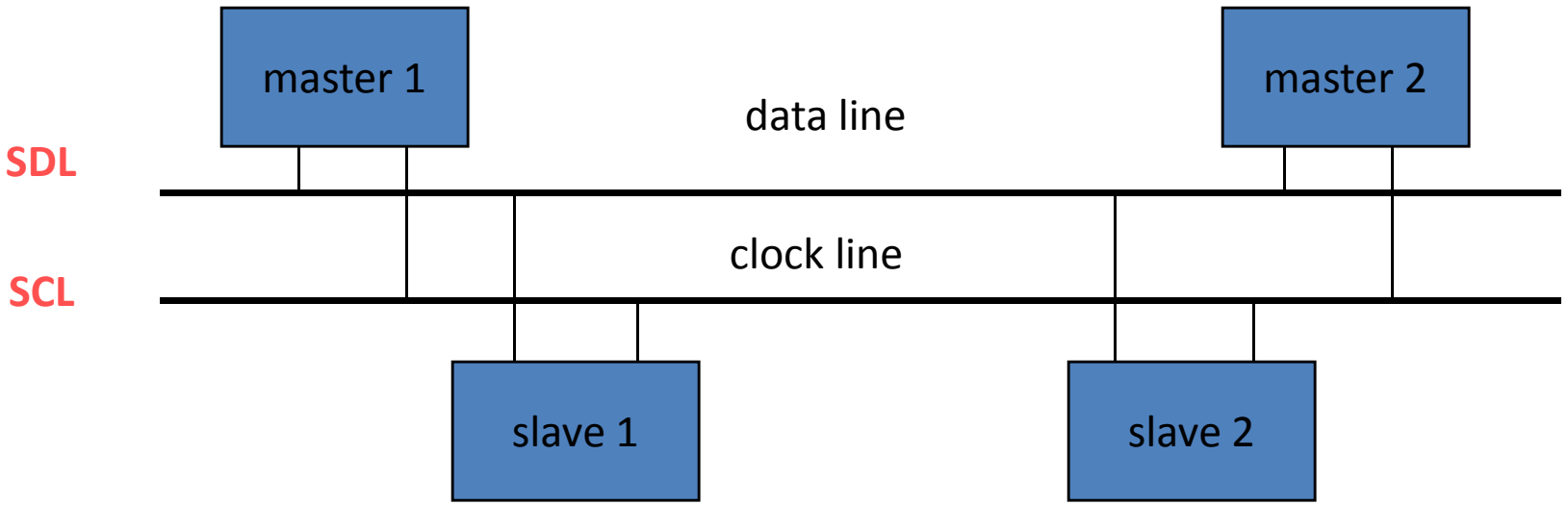
Logic analyzer architecture



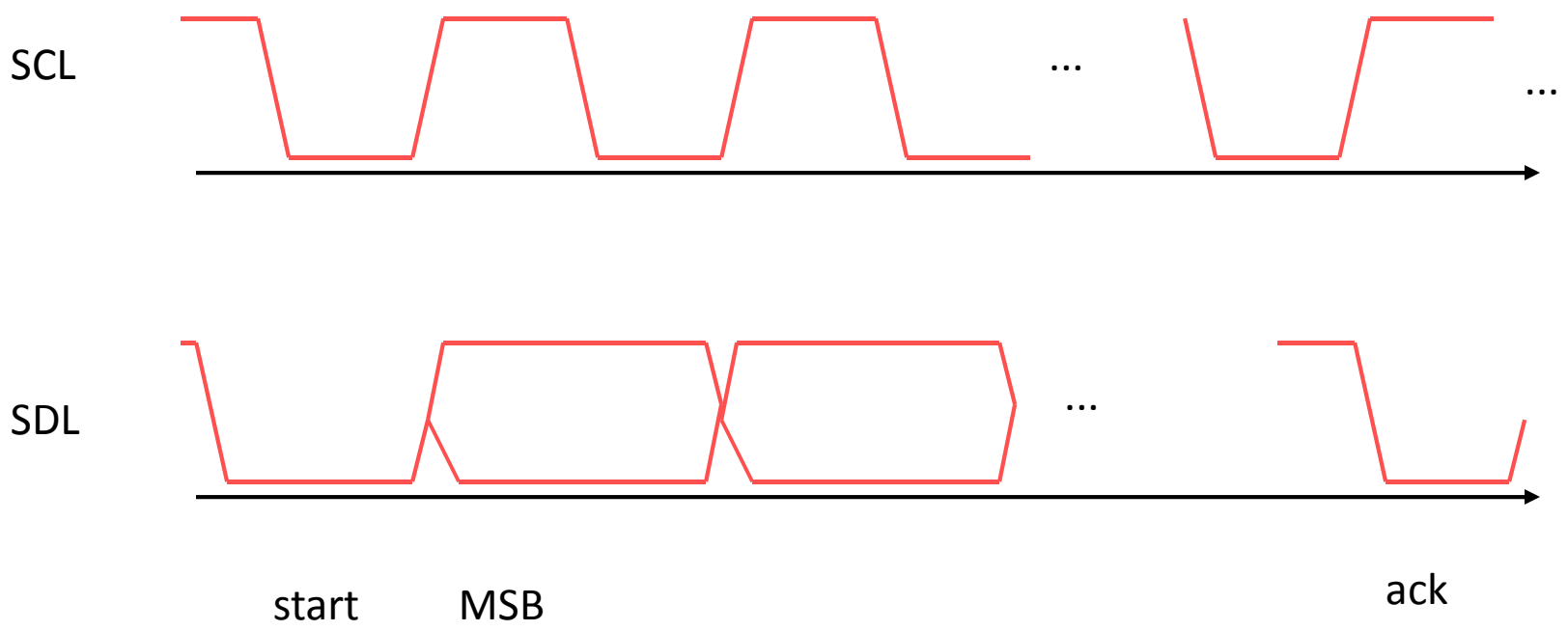
I^2C bus

- Designed for low-cost, medium data rate applications.
- Characteristics:
  - serial;
  - multiple-master;
  - fixed-priority arbitration.
- Several microcontrollers come with built-in I^2C controllers.

I²C physical layer

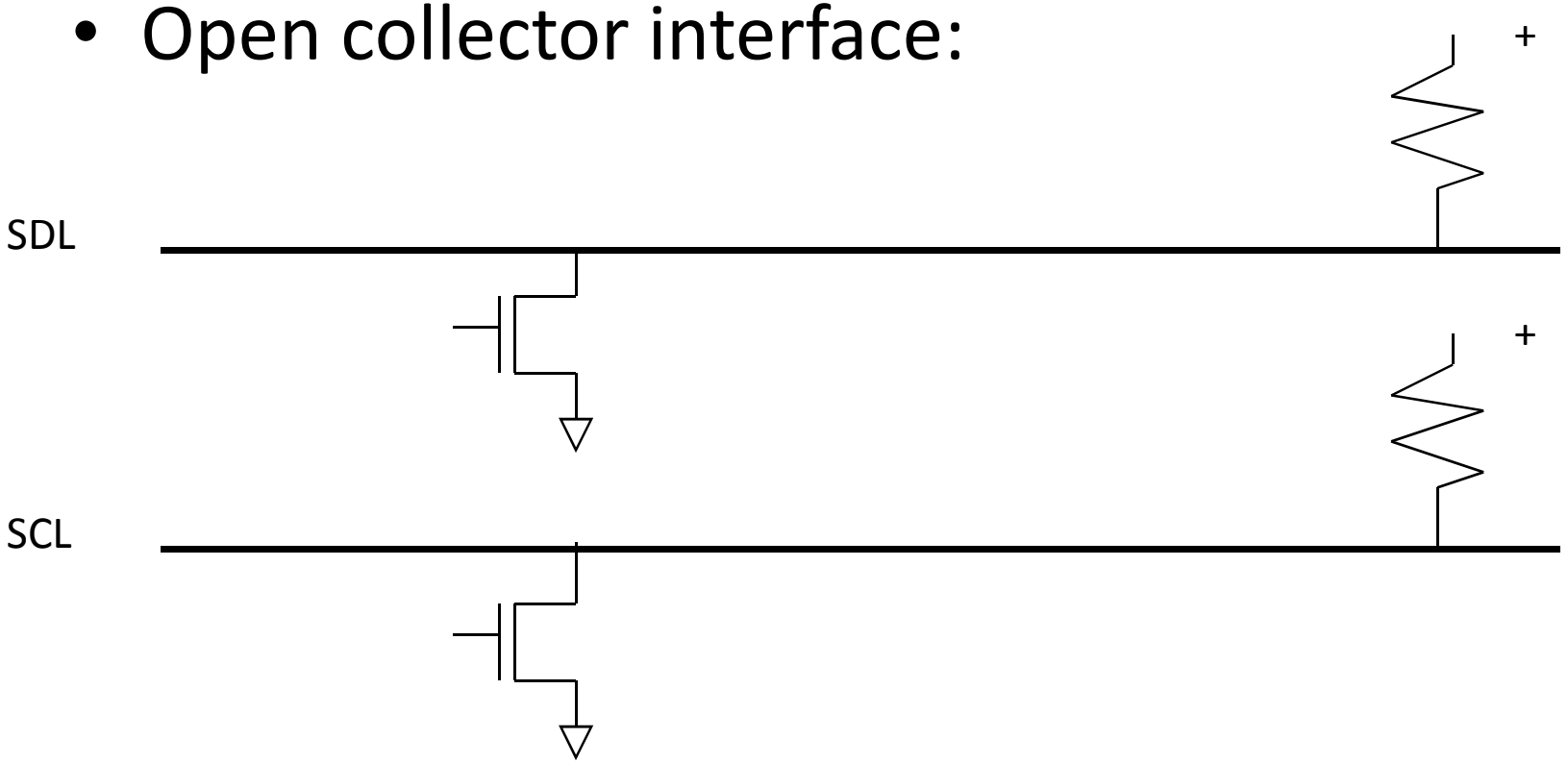


I²C data format



I^2C electrical interface

- Open collector interface:



I^2C signaling

- Sender pulls down bus for 0.
- Sender listens to bus---if it tried to send a 1 and heard a 0, someone else is simultaneously transmitting.
- Transmissions occur in 8-bit bytes.

I^2C data link layer

- Every device has an address (7 bits in standard, 10 bits in extension).
  - Bit 8 of address signals read or write.
- General call address allows broadcast.

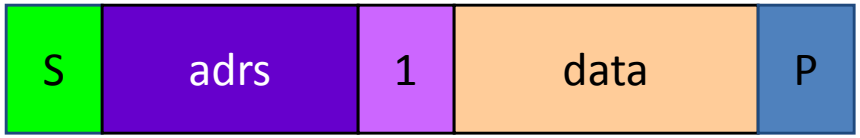
I^2C bus arbitration

- Sender listens while sending address.
- When sender hears a conflict, if its address is higher, it stops signaling.
- Low-priority senders relinquish control early enough in clock cycle to allow bit to be transmitted reliably.

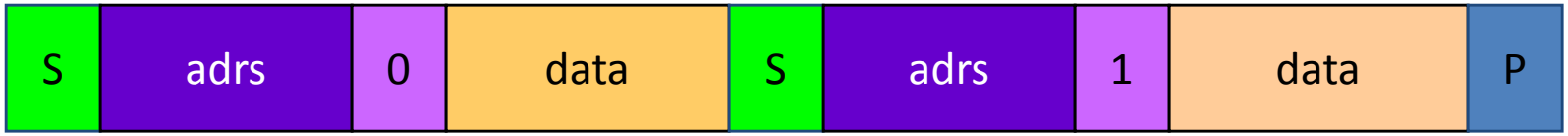
I²C transmissions

multi-byte write

read from slave



write, then read



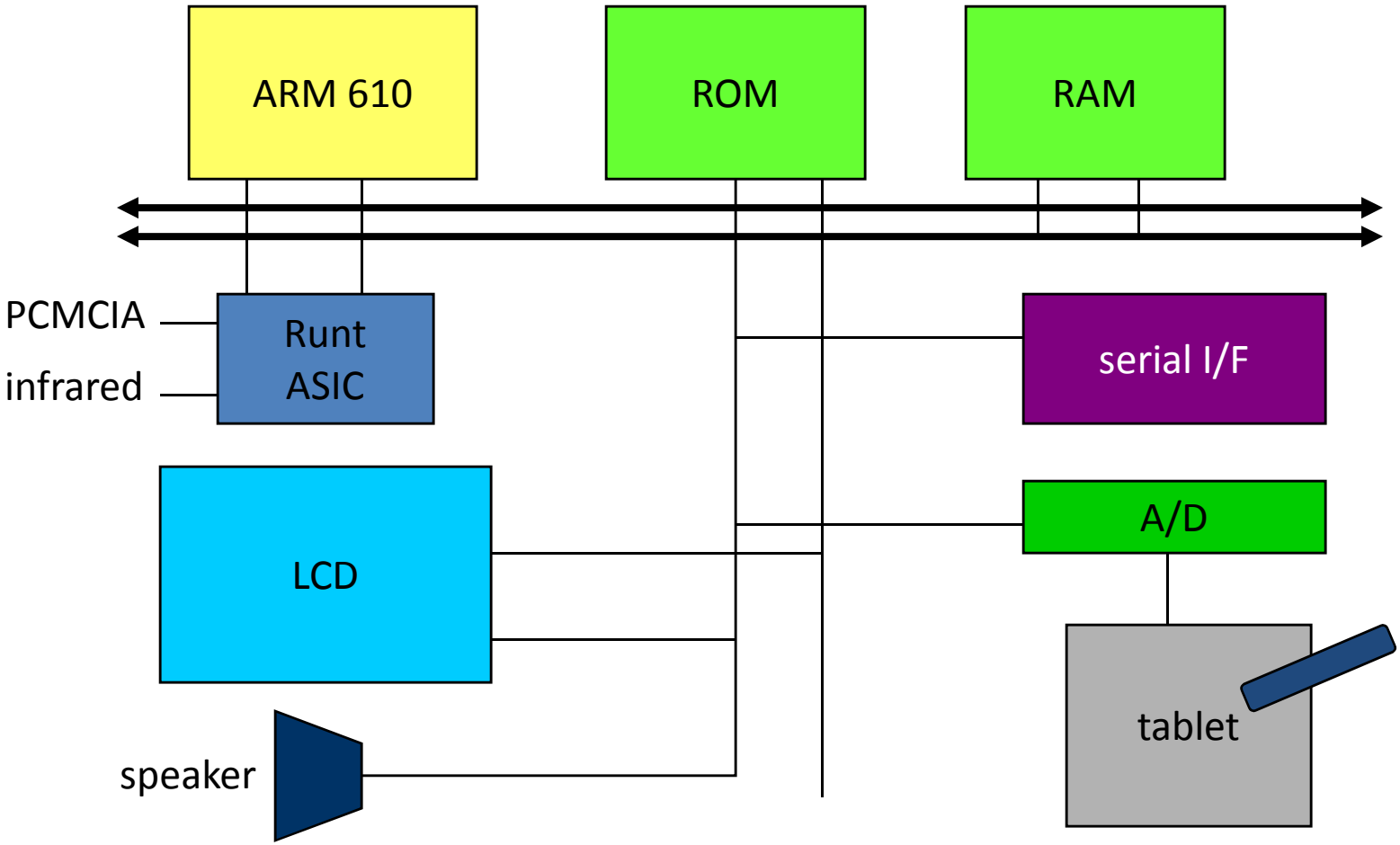
Personal digital assistant

- PDA: portable, specialized information device.
- Characteristics:
  - low cost for consumer market;
  - physically small;
  - battery-powered;
  - software-rich.

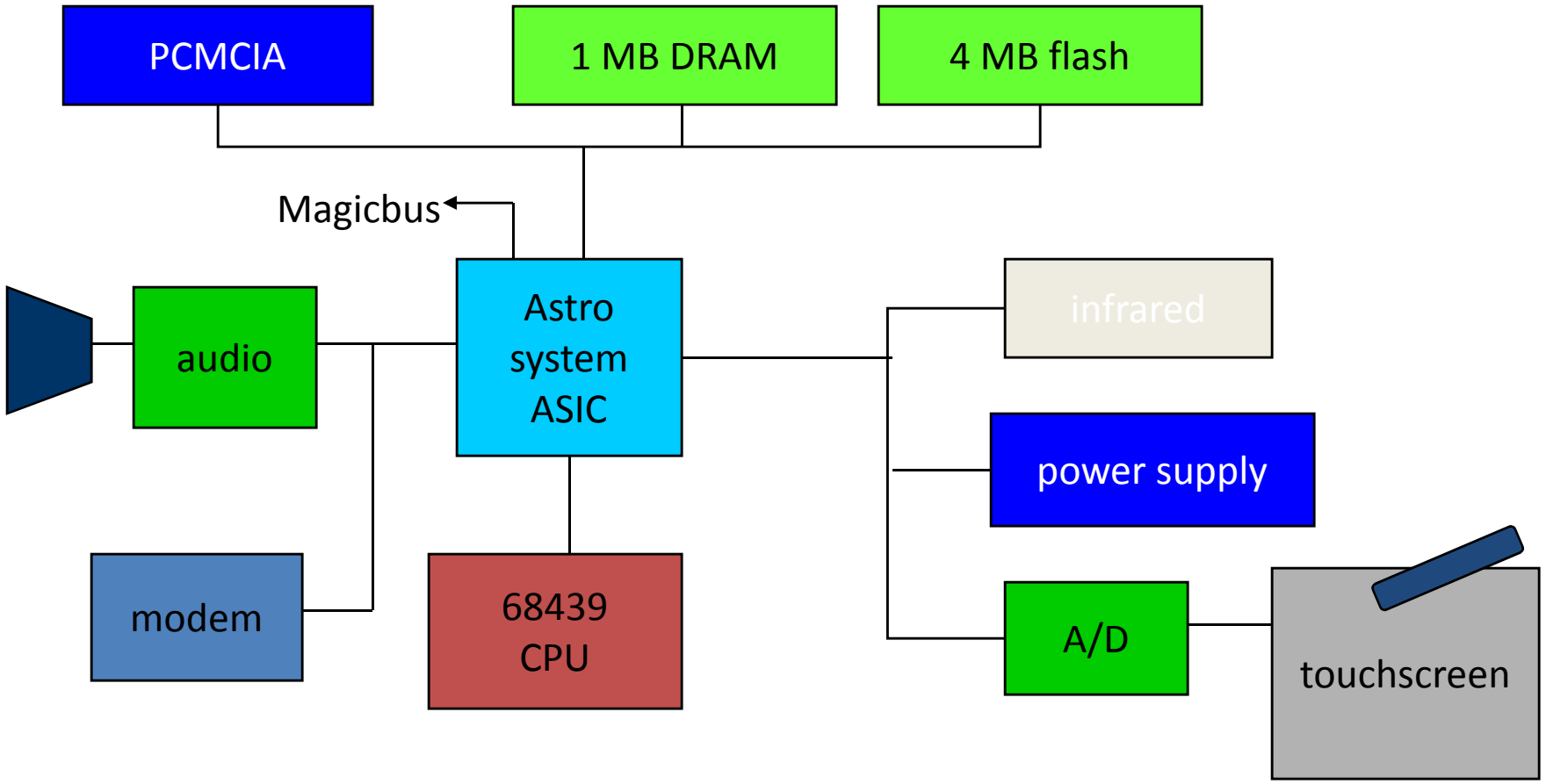
Apple Newton

- First modern PDA.
- Original used ARM 610; later version used StrongARM (ARM7) last: ARM9.
- Support operations in Runt ASIC: DMA, real-time clock, video interface, audio, PCMCIA.
- Software written in NewtonScript language.

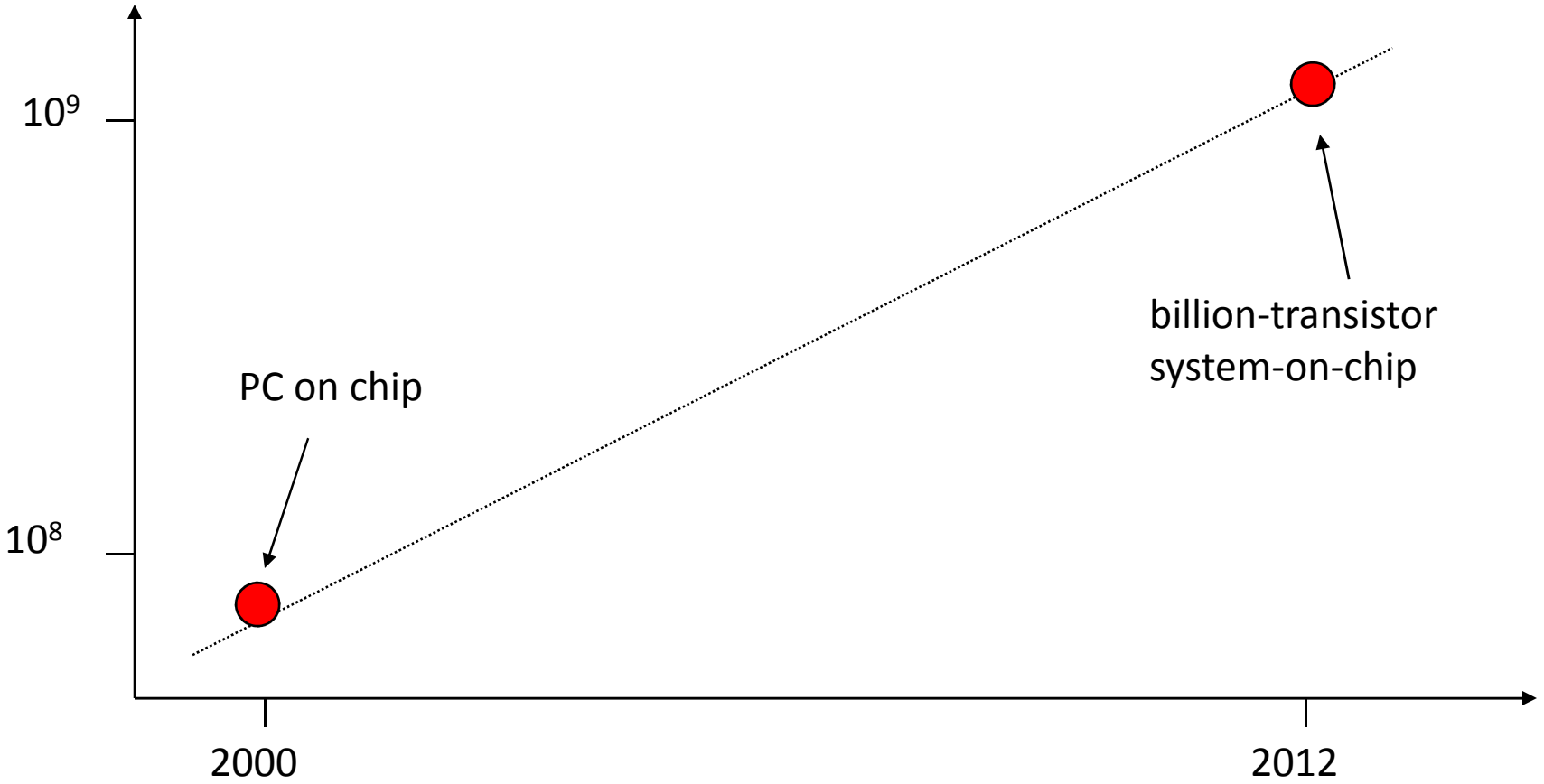
Newton hardware architecture



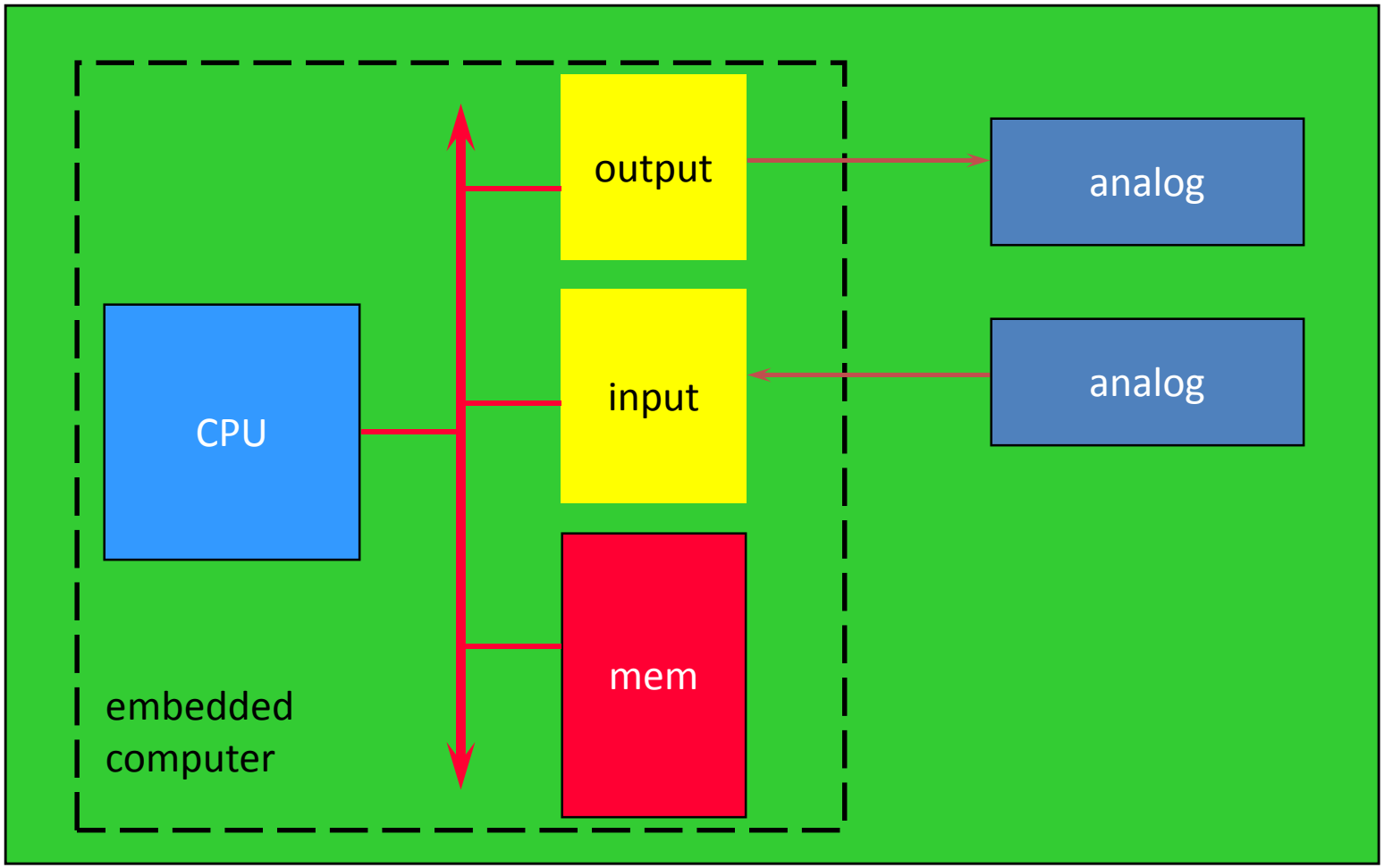
Motorola Envoy hardware architecture



Moore's Law (Sematech)



Embedding a computer



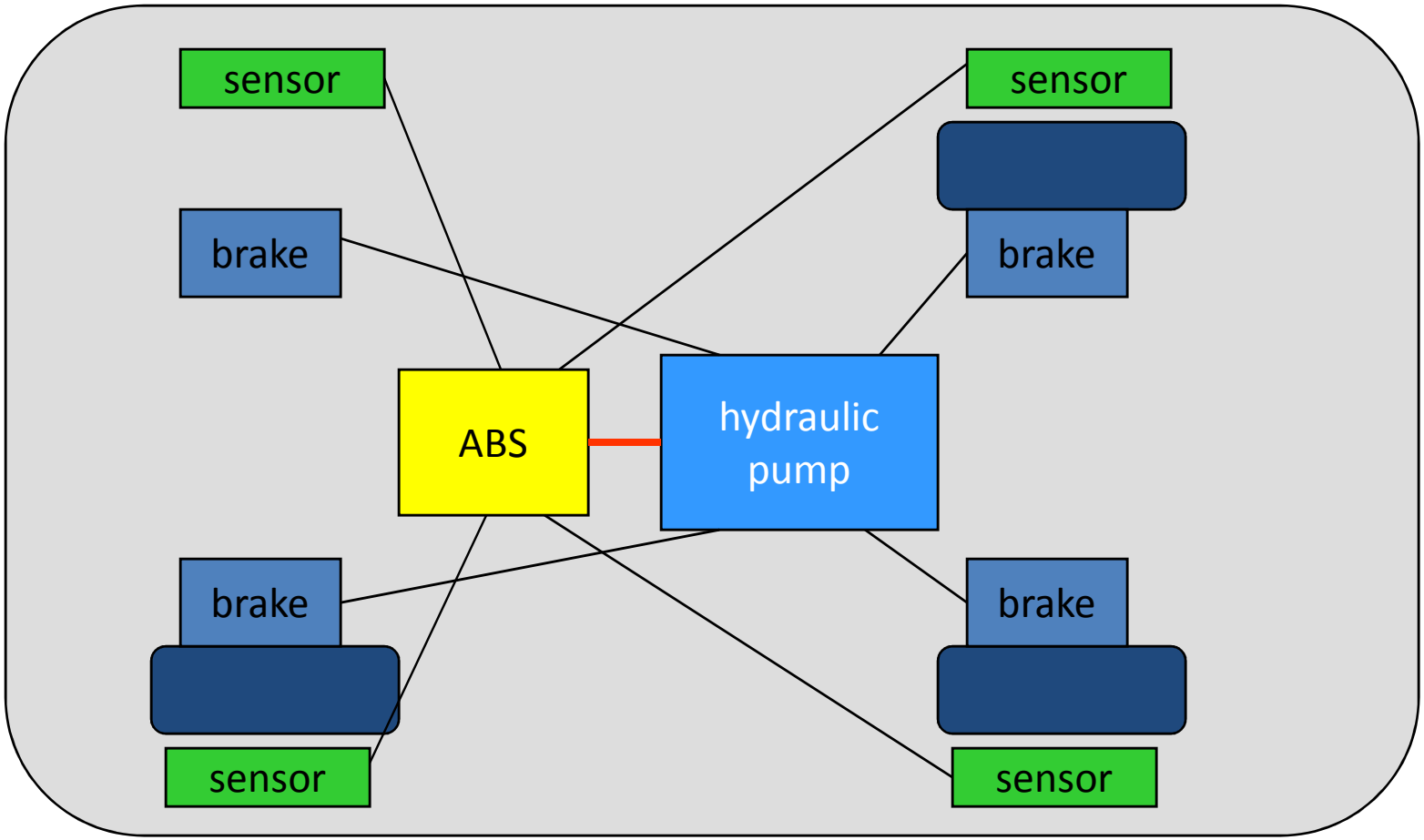
Examples

- Personal digital assistant (PDA).
- Printer.
- Cell phone.
- Automobile: engine, brakes, dash, etc.
- Television.
- Household appliances.
- PC keyboard (scans keys).

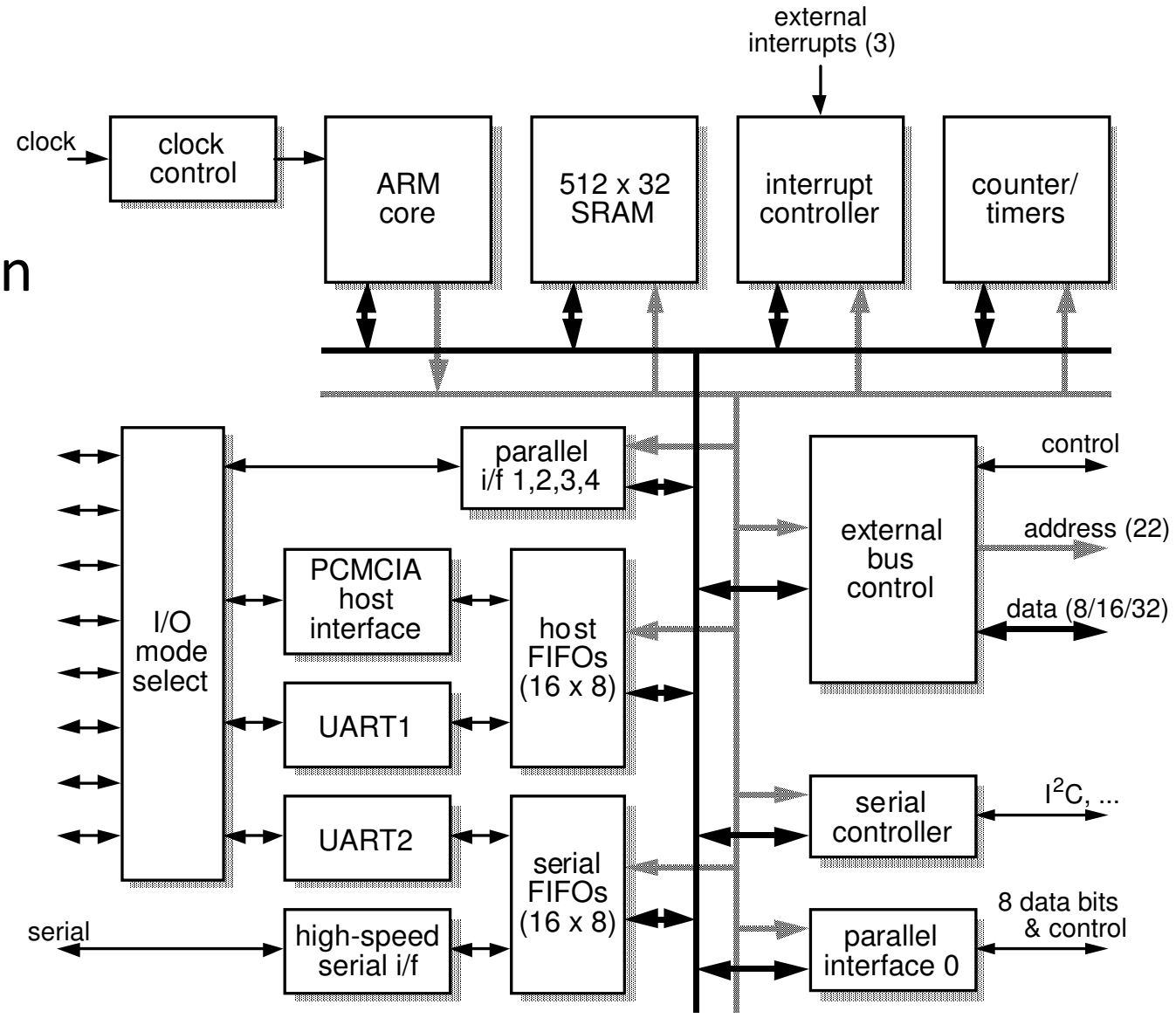
BMW 850i brake and stability control system

- Anti-lock brake system (ABS): pumps brakes to reduce skidding.
- Automatic stability control (ASC+T): controls engine to improve stability.
- ABS and ASC+T communicate.
  - ABS was introduced first---needed to interface to existing ABS module.

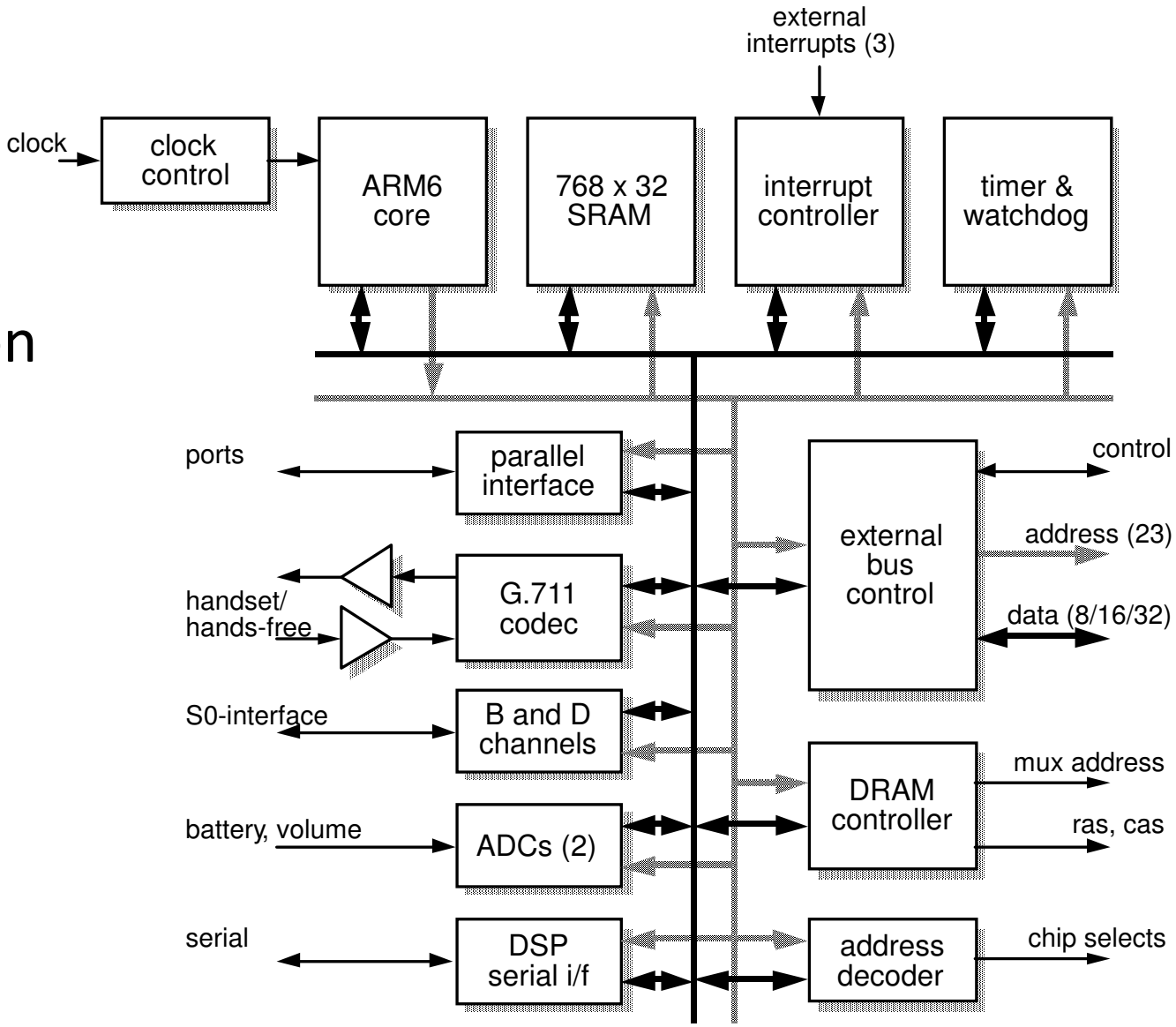
BMW 850i, cont'd.



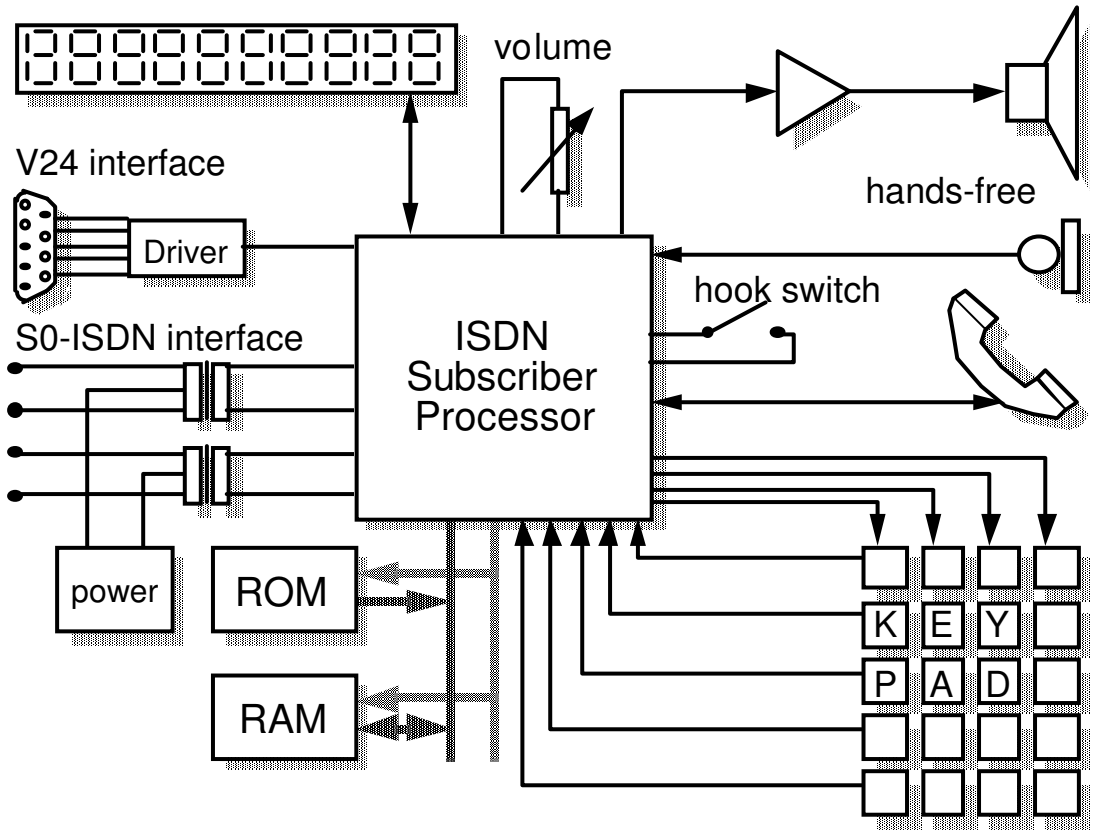
Ruby II advanced communication controller organization



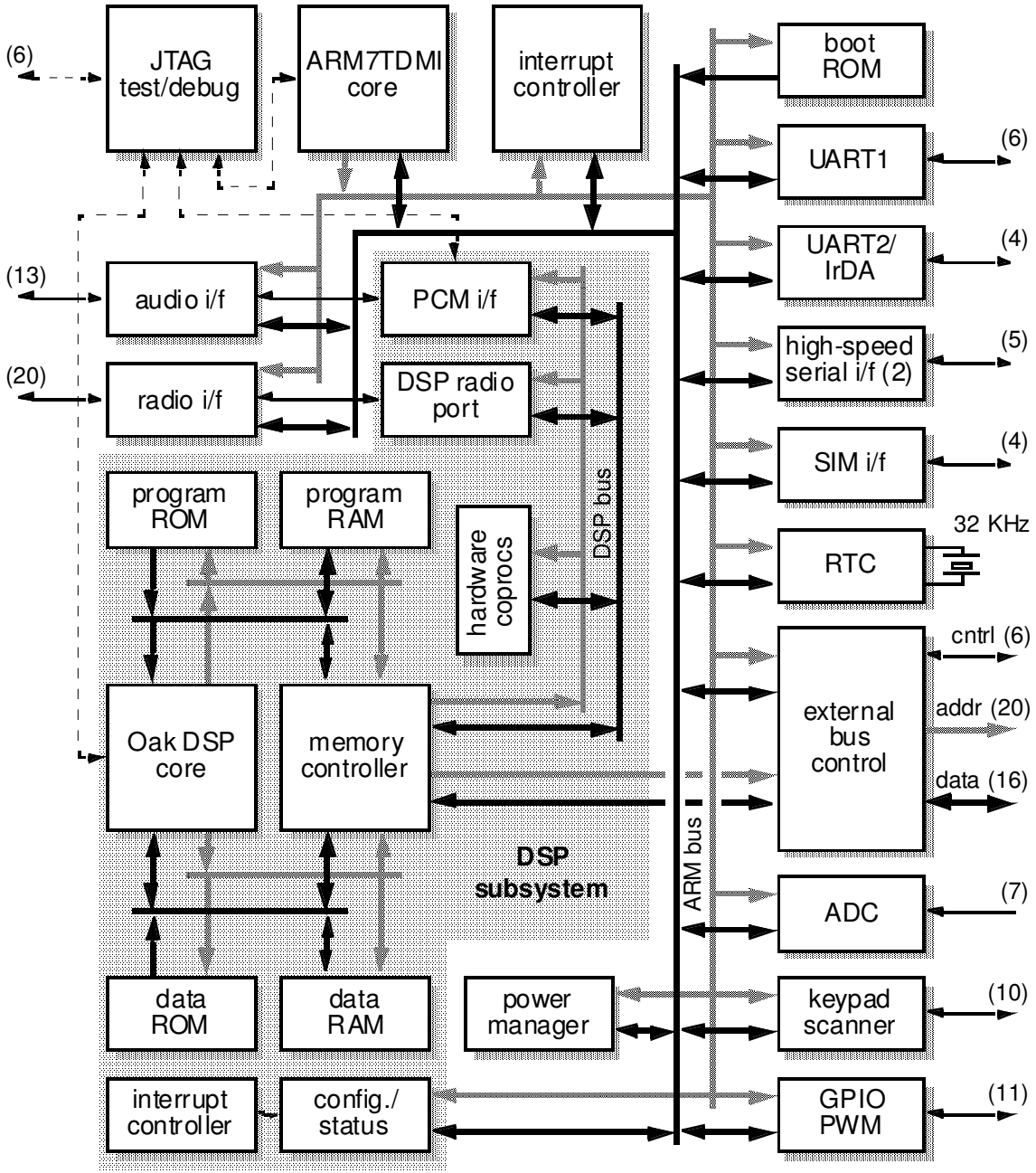
VIP organization



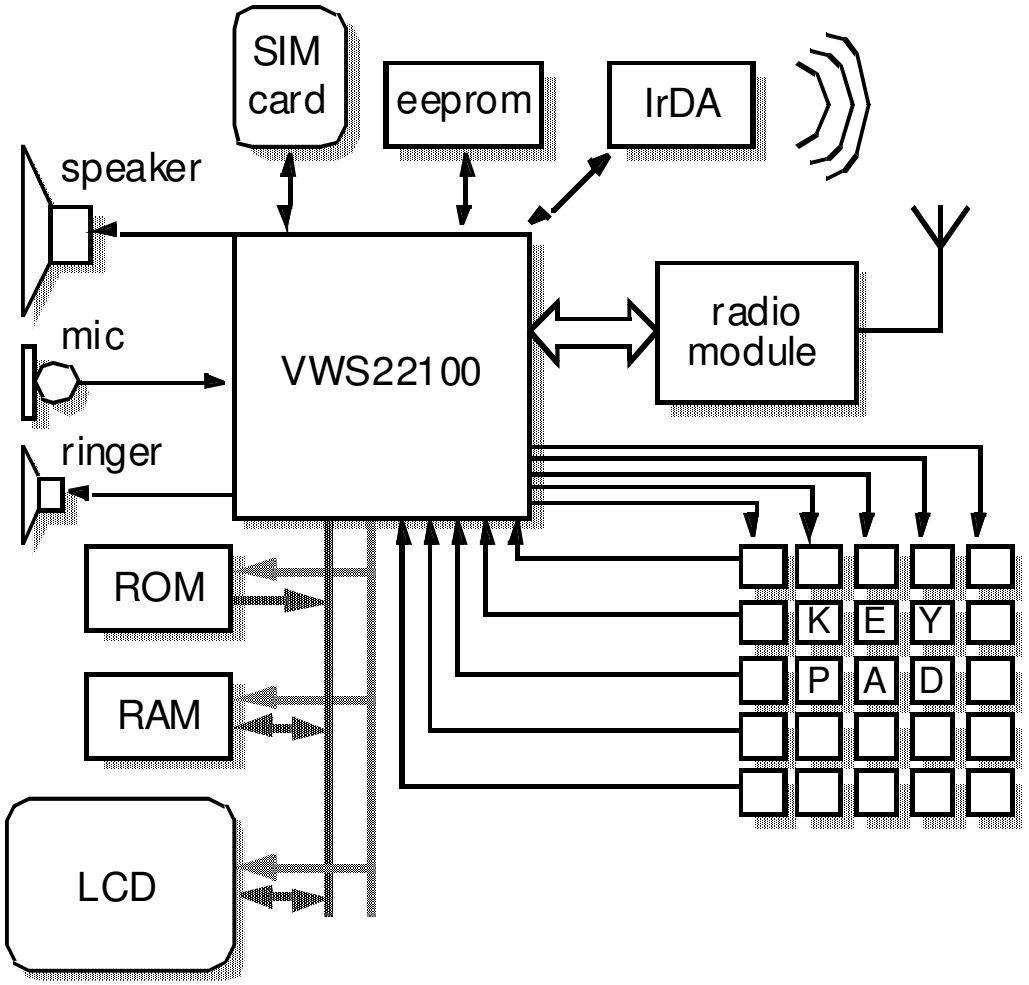
Typical VIP system configuration



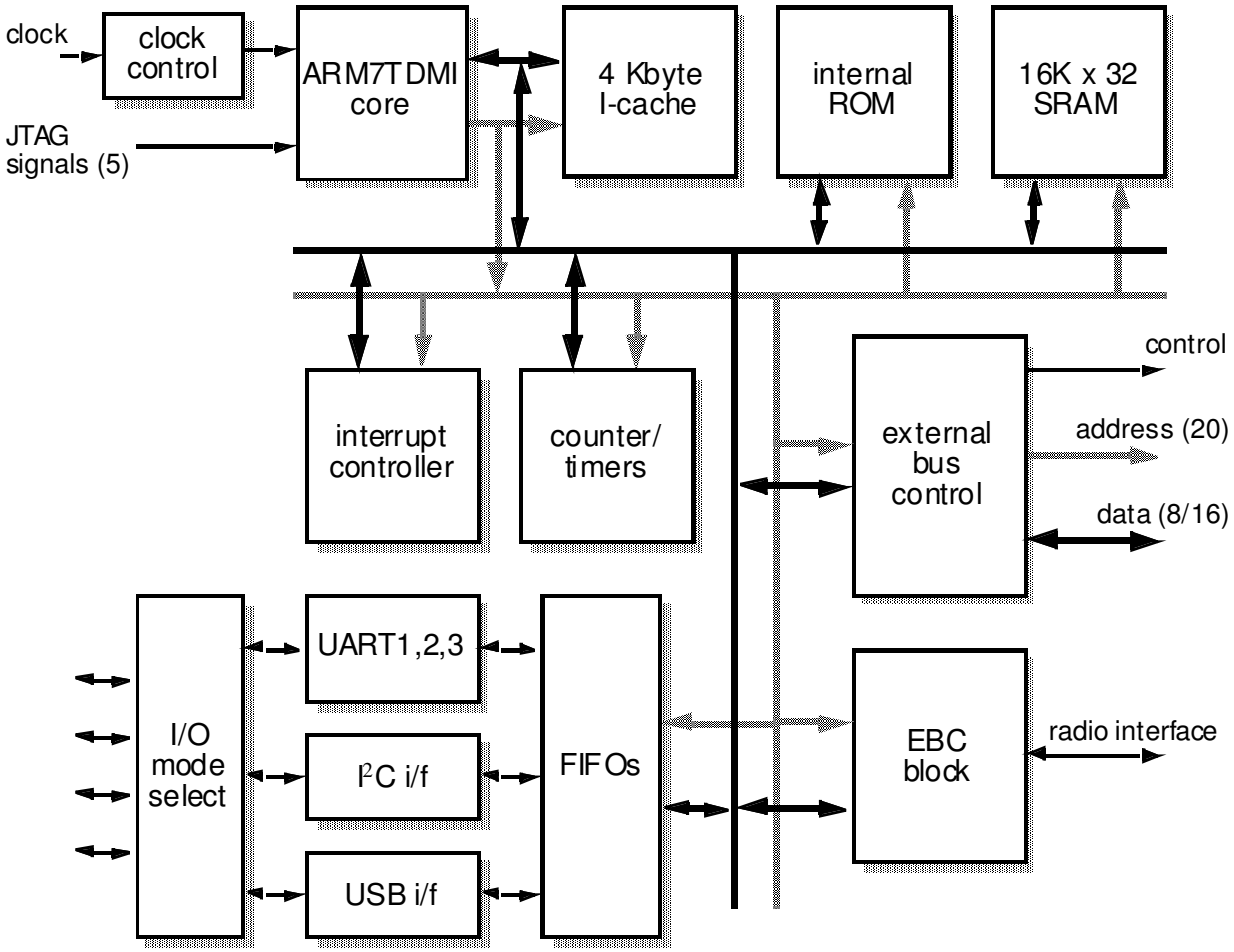
OneC VWS22100 GSM chip organization



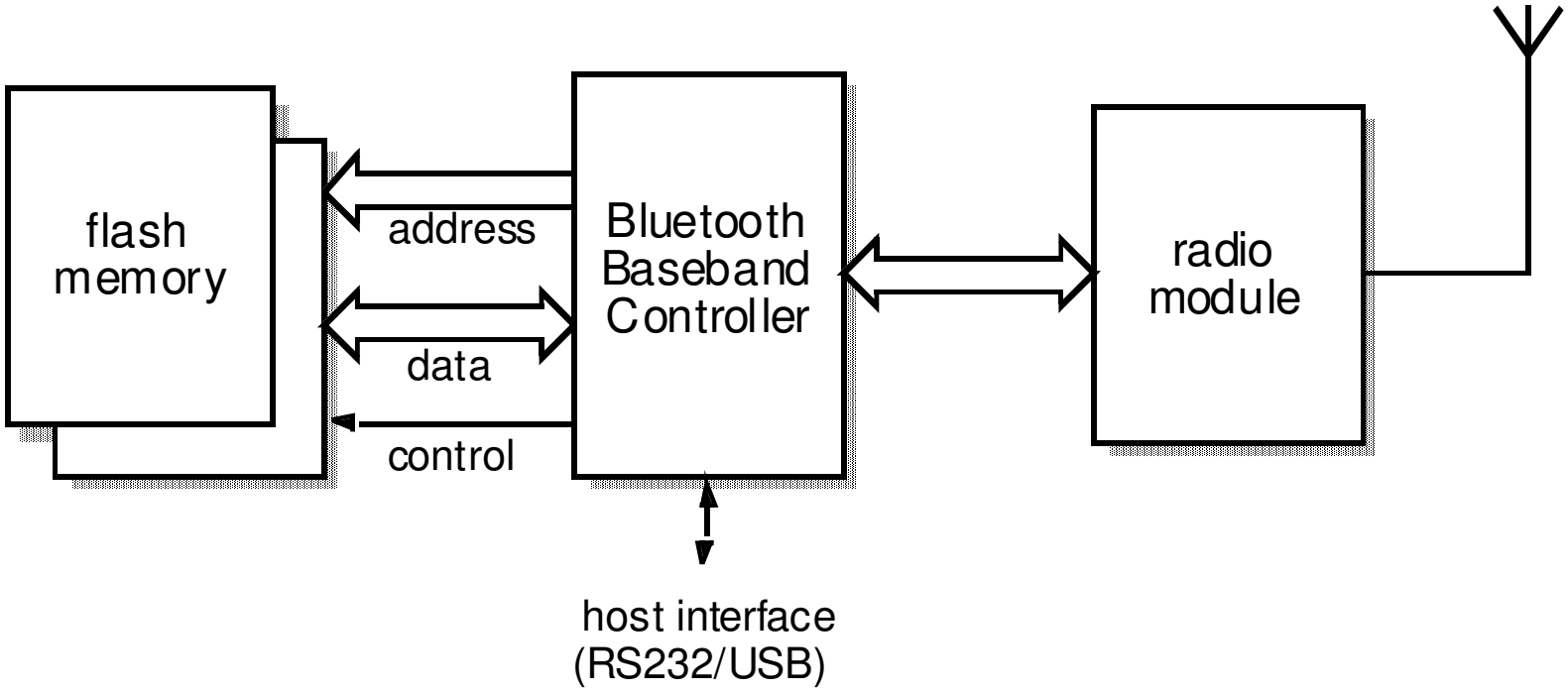
Typical GSM handset architecture



Ericsson-VLSI Bluetooth Baseband Controller organization



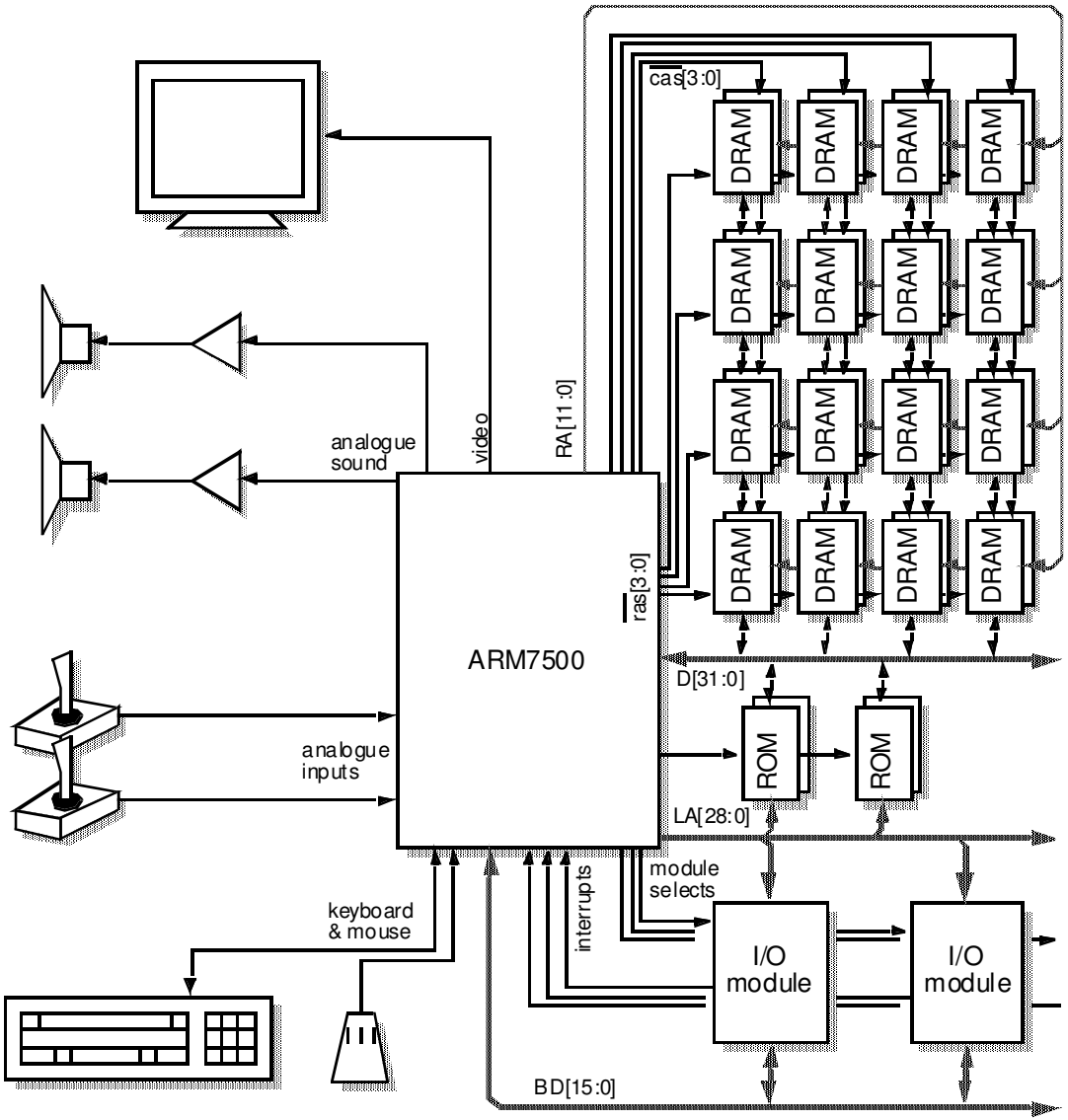
Typical Bluetooth application



Bluetooth characteristics

Process	0.25 um	**Transistors**	4,300,000	**MIPS**	12
Metal layers	3	**Die area**	20 mm^2	**Power**	75 mW
Vdd	2.5 V	**Clock**	0 – 13 MHz	**MIPS/W**	160

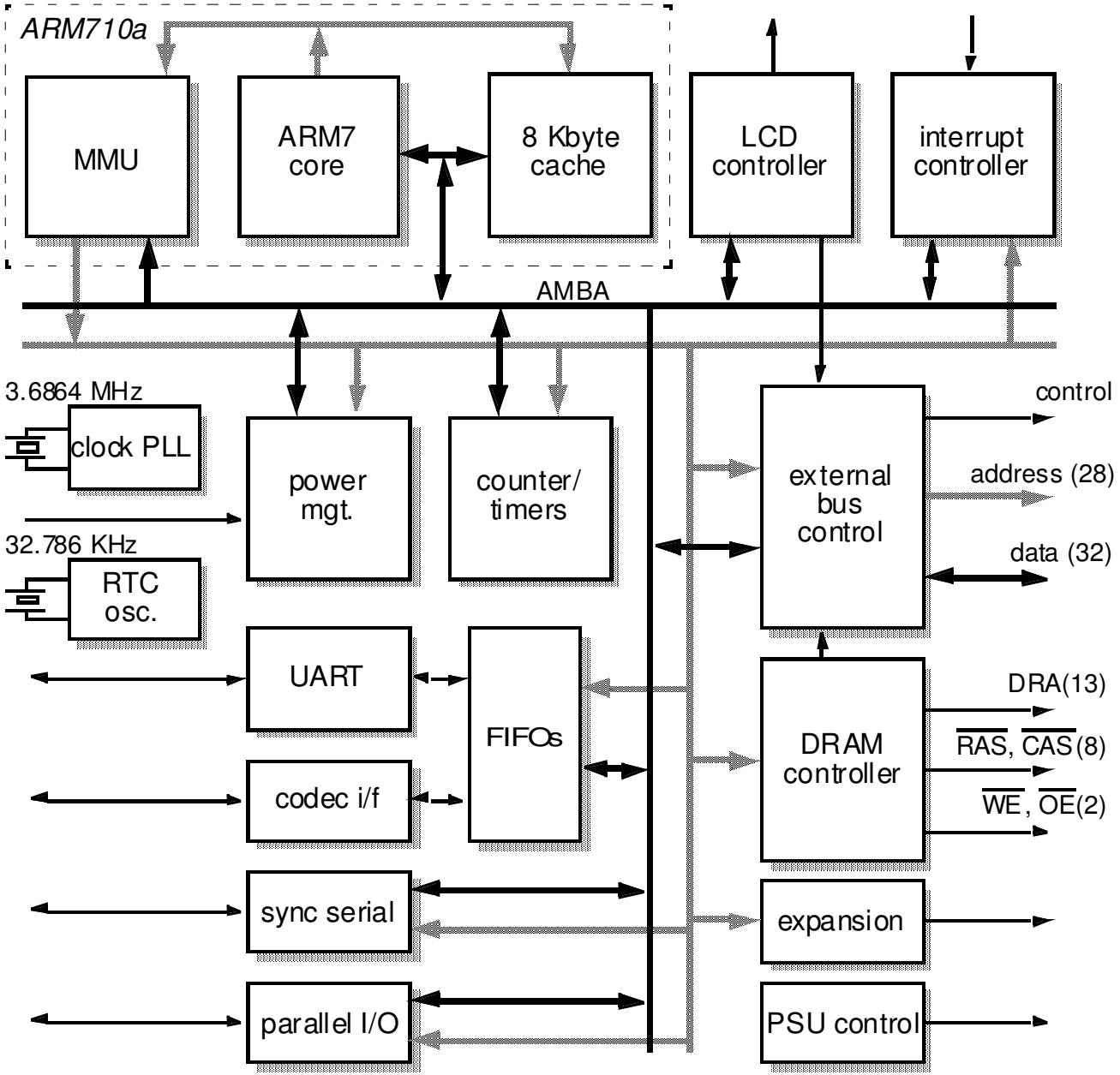
Typical ARM7500 system organization



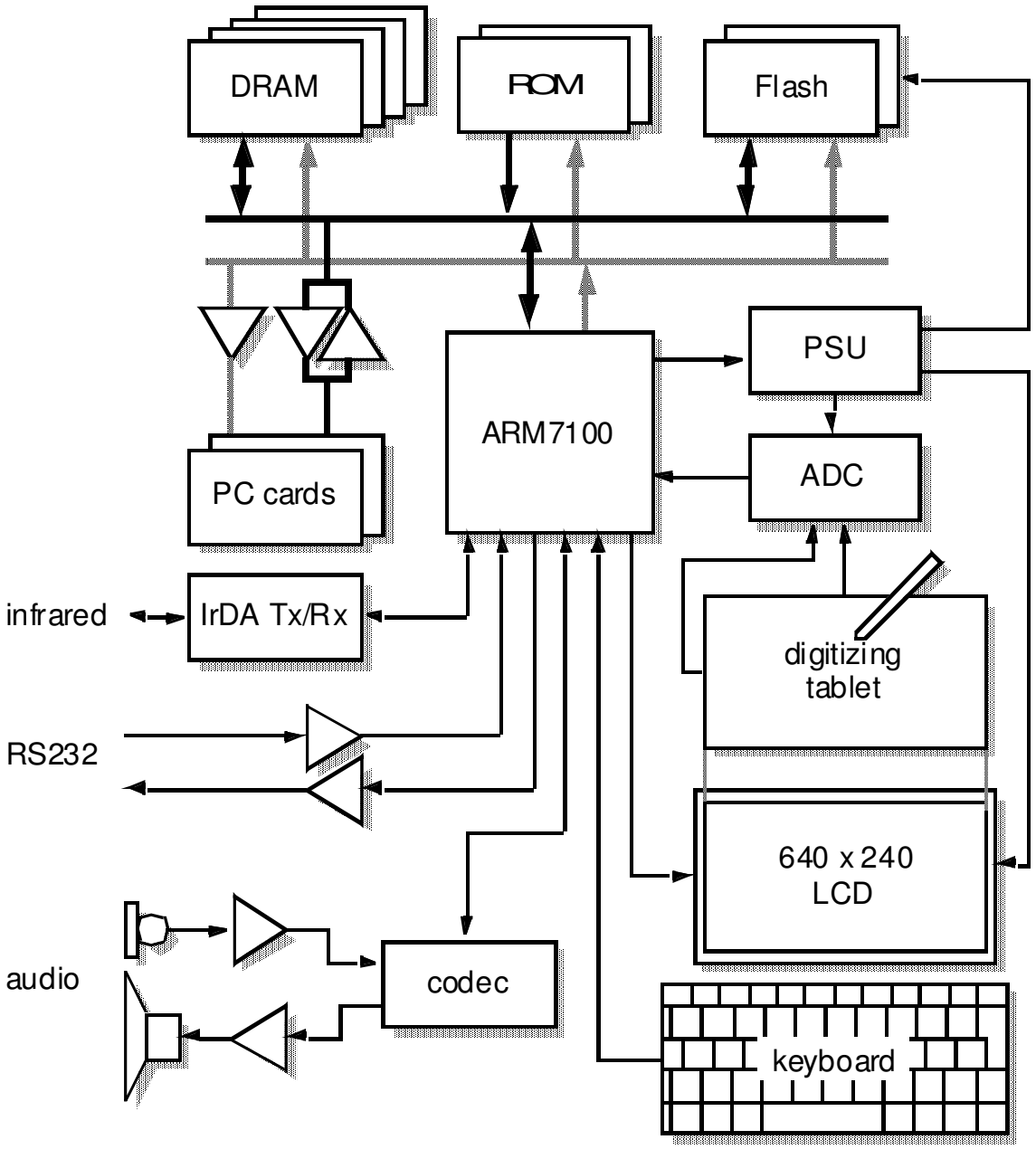
ARM7500 characteristics

Process	0.6 um	**Transistors**	550,000	**MIPS**	30
Metal layers	2	**Die area**	70 mm^2	**Power**	690 mW
Vdd	5 V	**Clock**	0 to 33 MHz	**MIPS/W**	43

ARM7100 organization



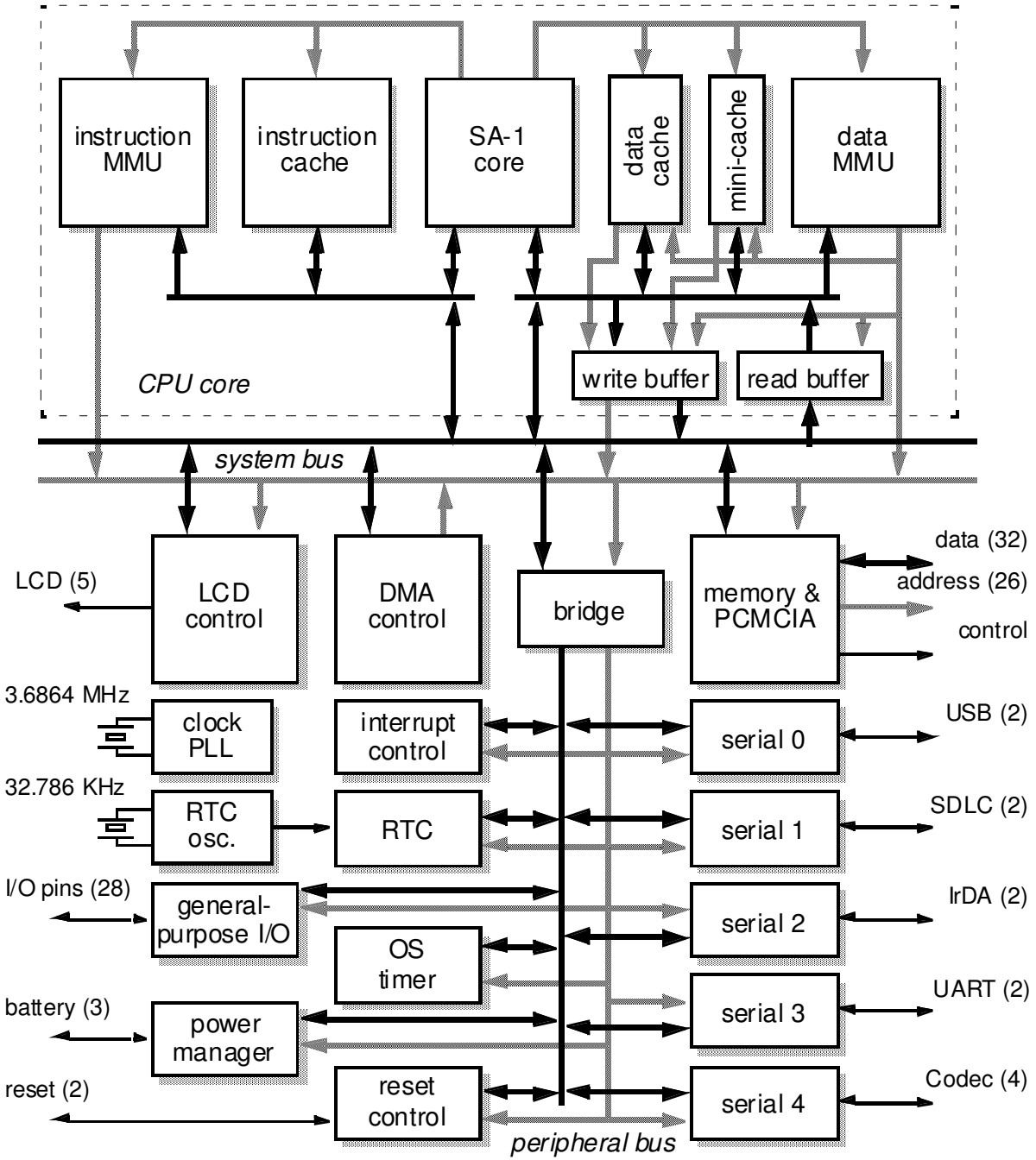
The Psion Series 5 hardware organization



ARM7100 characteristics

Process	0.6 um	**Transistors**	N/A	**MIPS**	30
Metal layers	2	**Die area**	N/A mm^2	**Power**	14 mW
Vdd	3.3 V	**Clock**	18.432 MHz	**MIPS/W**	212

SA-1100 organization



SA-1100 characteristics

Process	0.35 um	**Transistors**	2,500,000	**MIPS**	220/250
Metal layers	3	**Die area**	75 mm^2	**Power**	330/550 mW
Vdd	1.5/2 V	**Clock**	190/220 MHz	**MIPS/W**	665/450