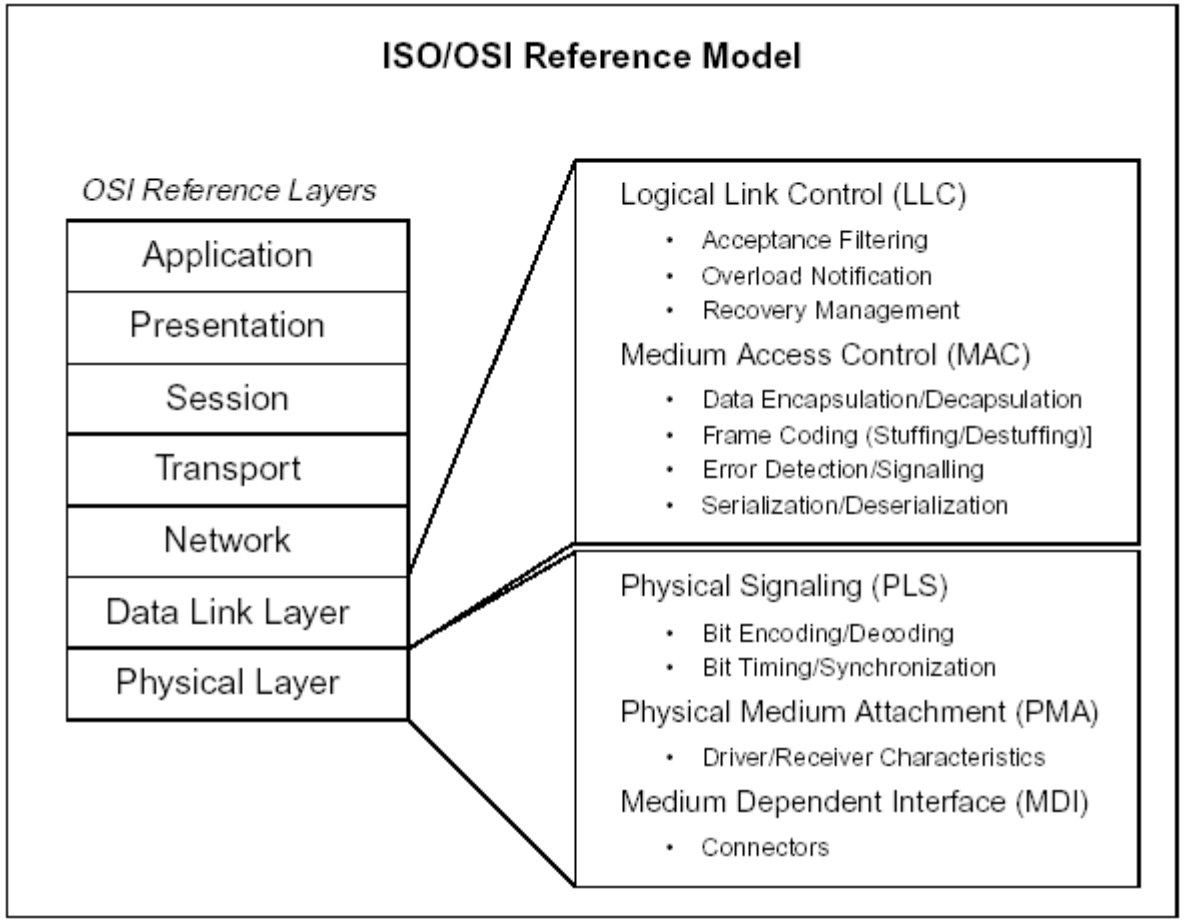
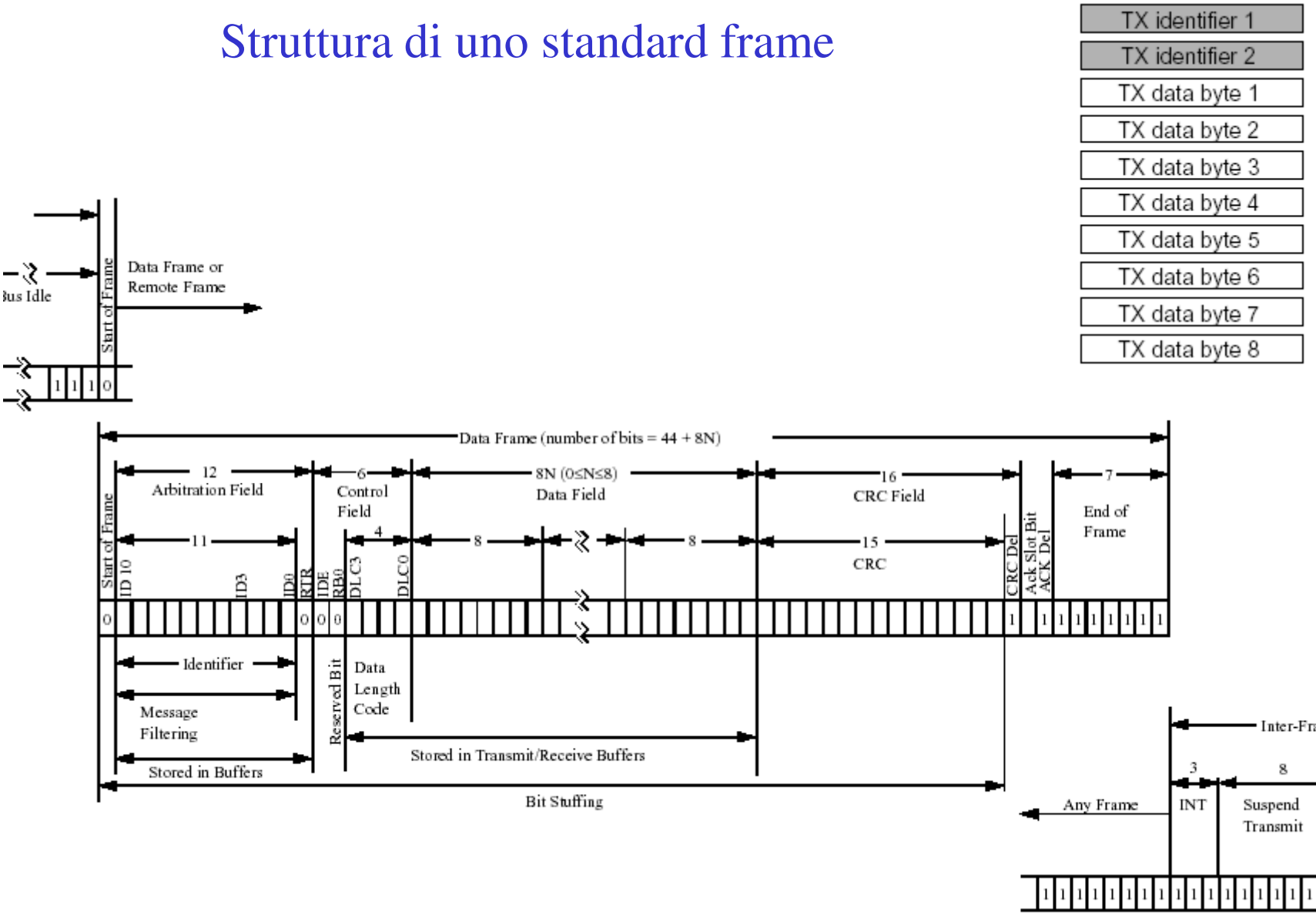
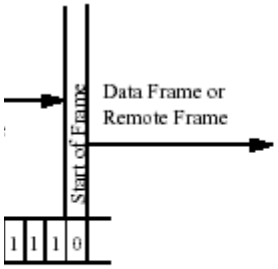
# Modello ISO-OSI e Livelli specificati dalla norma SAE J1939

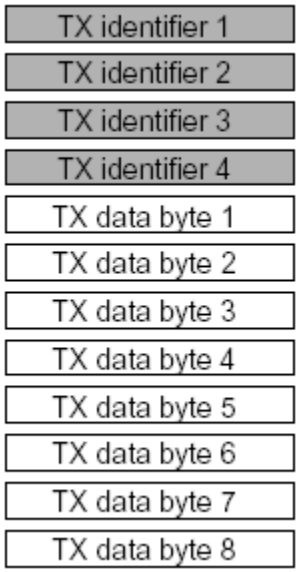


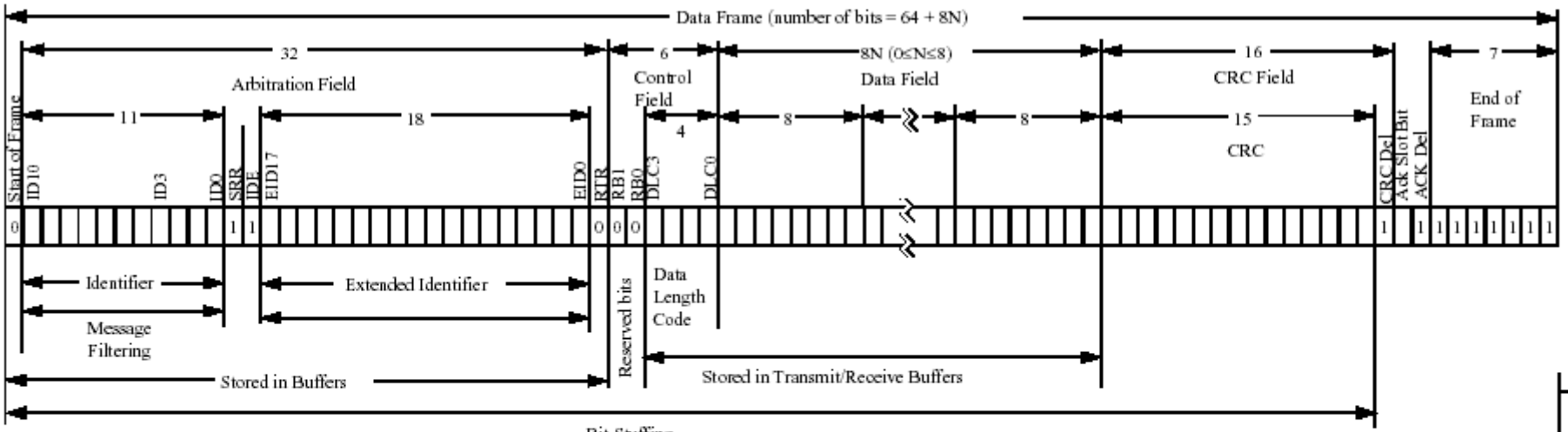
# Struttura di uno standard frame

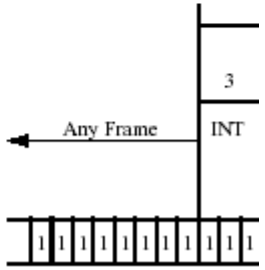


# Struttura di un extended frame



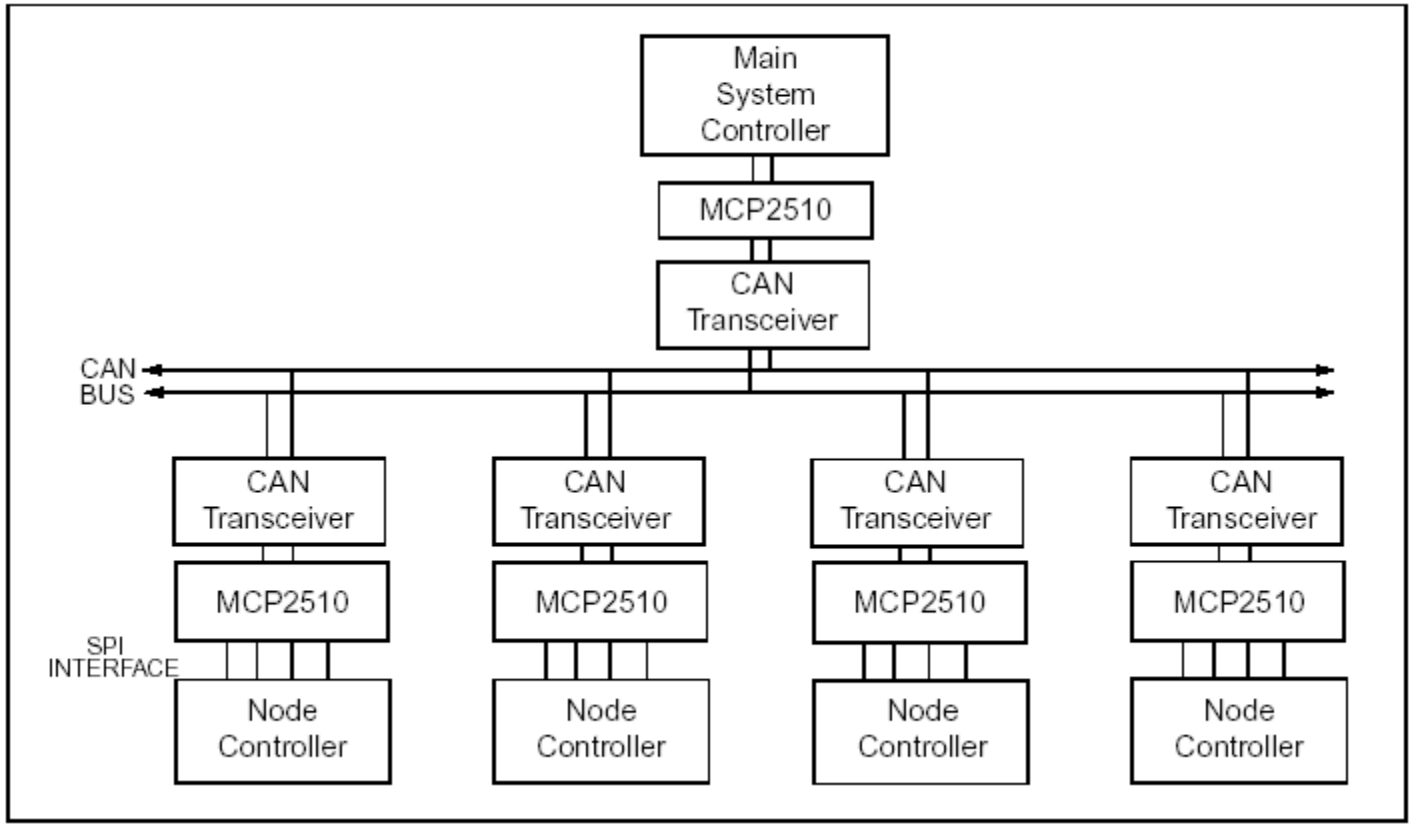



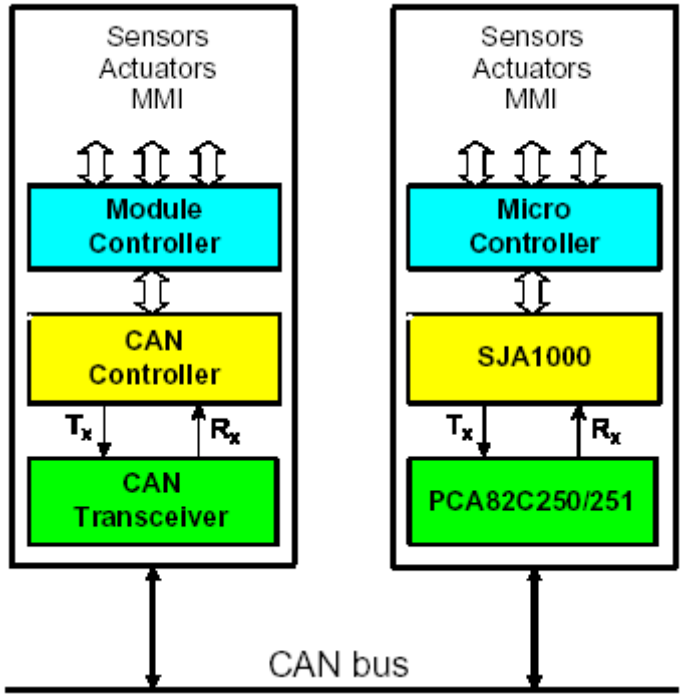
Tipica implementazione di rete CAN singola

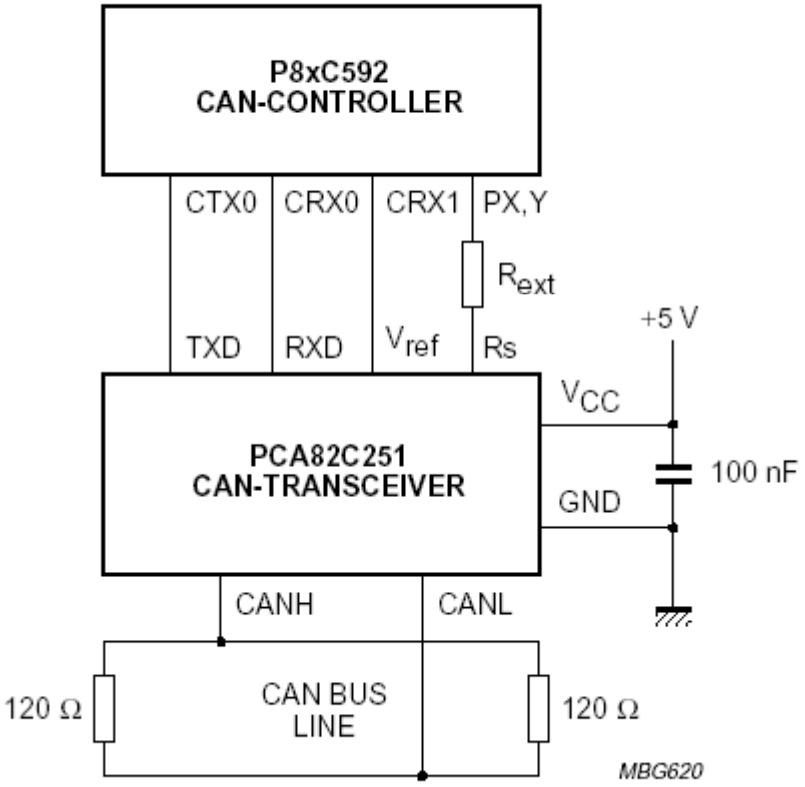
Per ogni nodo è presente:

- un CAN controller (come SJA100 oppure MCP2510) e
- un CAN Transceiver (come PCA82C251 Philips)



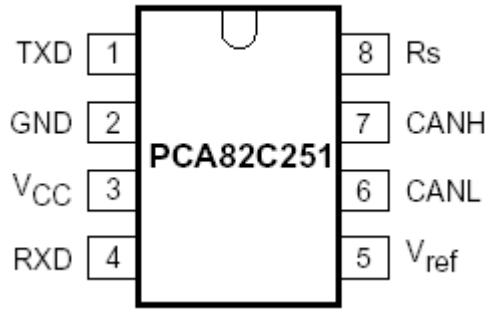
# Tipica implementazione di rete CAN singola: singolo nodo



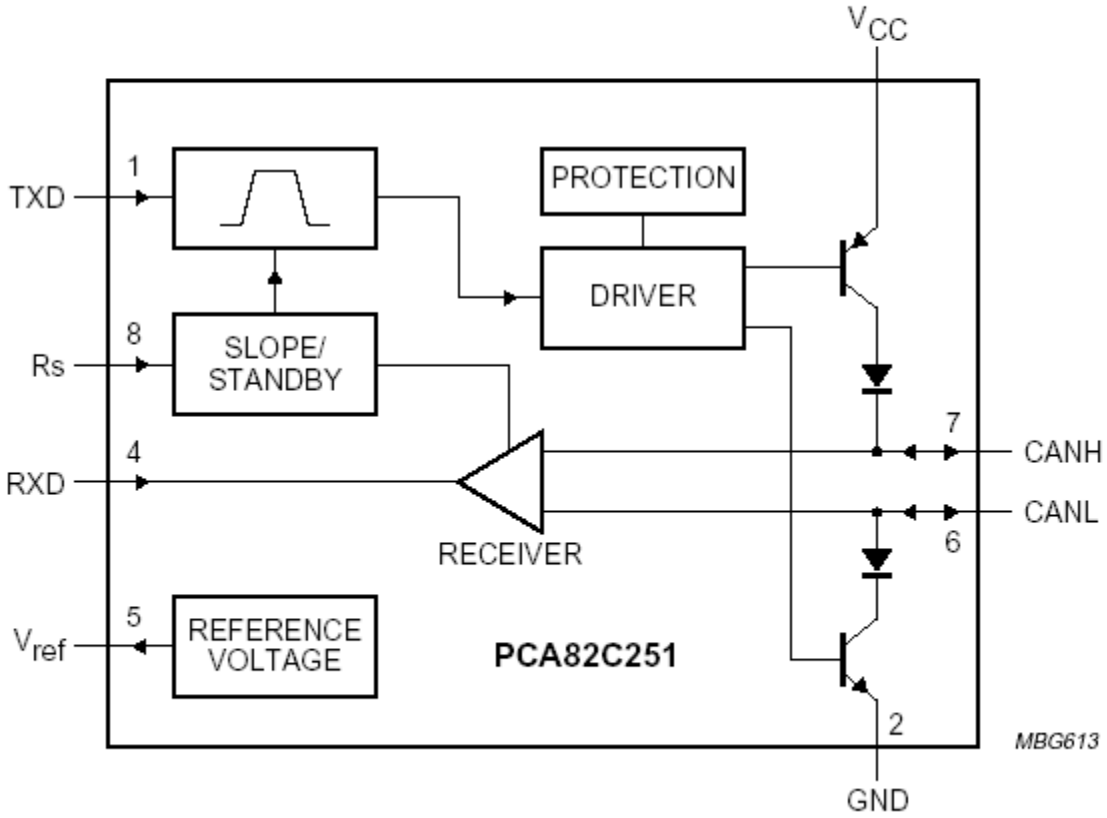



# Il CAN Transceiver PCA82C251 Philips:

## Pinout e diagramma a blocchi interno




| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| TXD | 1 | transmit data input |
| GND | 2 | ground |
| $V_{CC}$ | 3 | supply voltage |
| RXD | 4 | receive data output |
| $V_{ref}$ | 5 | reference voltage output |
| CANL | 6 | LOW level CAN voltage input/output |
| CANH | 7 | HIGH level CAN voltage input/output |
| Rs | 8 | slope resistor input |



# Philips SJA1000 CAN Controller: Diagramma a Blocchi

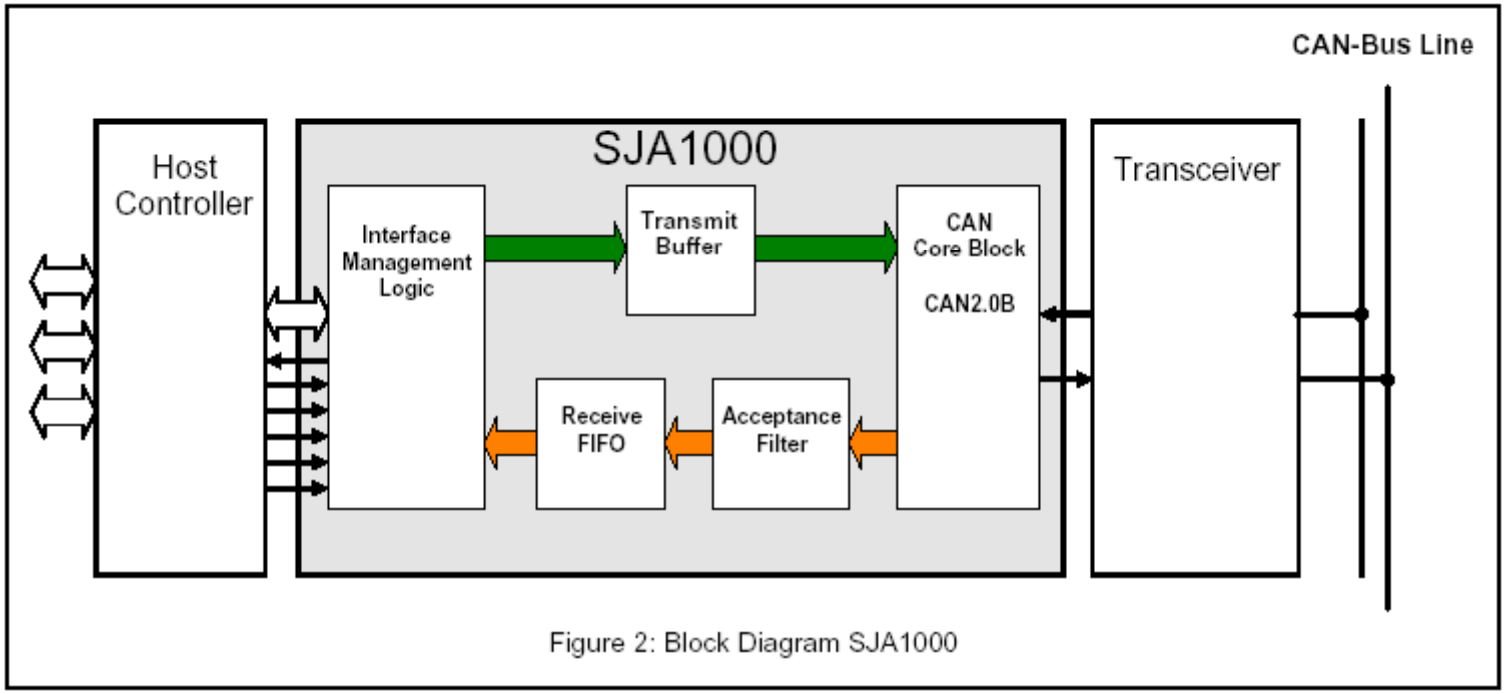
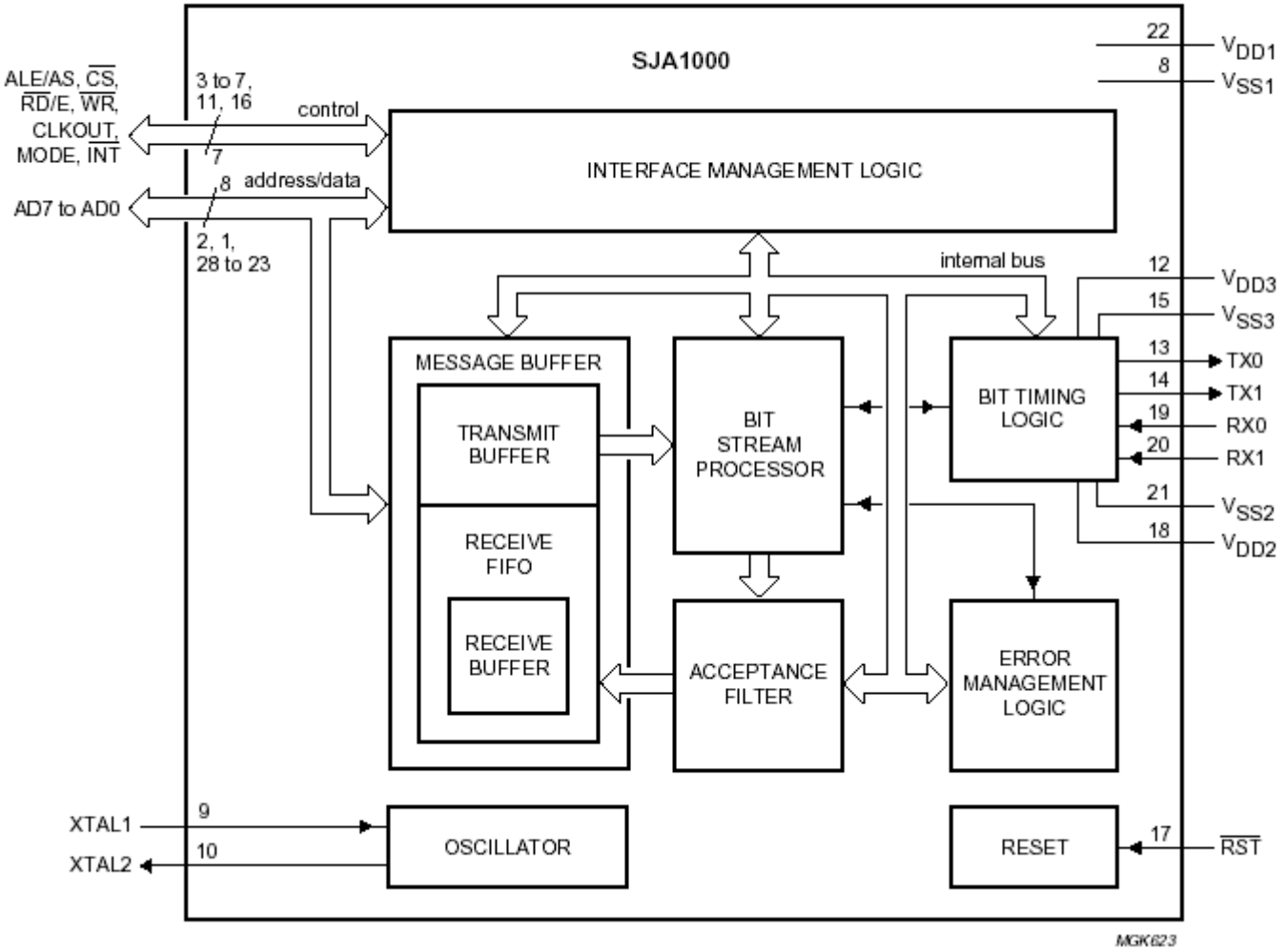
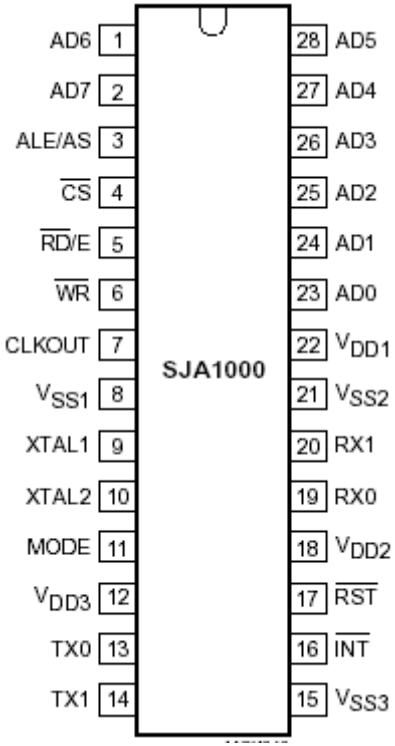



Figure 2: Block Diagram SJA1000

# Philips SJA1000 CAN Controller: Diagramma a Blocchi e pinout



# Philips SJA1000 CAN Controller: Pinout




| SYMBOL | PIN | DESCRIPTION |
|---|---|---|
| AD7 to AD0 | 2, 1, 28 to 23 | multiplexed address/data bus |
| ALE/AS | 3 | ALE input signal (Intel mode), AS input signal (Motorola mode) |
| $\overline{CS}$ | 4 | chip select input, LOW level allows access to the SJA1000 |
| $\overline{RD}$/E | 5 | $\overline{RD}$ signal (Intel mode) or E enable signal (Motorola mode) from the microcontroller |
| $\overline{WR}$ | 6 | $\overline{WR}$ signal (Intel mode) or RD/$\overline{WR}$ signal (Motorola mode) from the microcontroller |
| CLKOUT | 7 | clock output signal produced by the SJA1000 for the microcontroller; the clock signal is derived from the built-in oscillator via the programmable divider; the clock off bit within the clock divider register allows this pin to disable |
| $V_{SS1}$ | 8 | ground for logic circuits |
| XTAL1 | 9 | input to the oscillator amplifier; external oscillator signal is input via this pin; note 1 |
| XTAL2 | 10 | output from the oscillator amplifier; the output must be left open-circuit when an external oscillator signal is used; note 1 |
| MODE | 11 | mode select input<br>1 = selects Intel mode<br>0 = selects Motorola mode |
| $V_{DD3}$ | 12 | 5 V supply for output driver |
| TX0 | 13 | output from the CAN output driver 0 to the physical bus line |
| TX1 | 14 | output from the CAN output driver 1 to the physical bus line |
| $V_{SS3}$ | 15 | ground for output driver |
| $\overline{INT}$ | 16 | interrupt output, used to interrupt the microcontroller; $\overline{INT}$ is active LOW if any bit of the internal interrupt register is set; $\overline{INT}$ is an open-drain output and is designed to be a wired-OR with other $\overline{INT}$ outputs within the system; a LOW level on this pin will reactivate the IC from sleep mode |
| $\overline{RST}$ | 17 | reset input, used to reset the CAN interface (active LOW); automatic power-on reset can be obtained by connecting $\overline{RST}$ via a capacitor to $V_{SS}$ and a resistor to $V_{DD}$ (e.g. C = 1 µF; R = 50 kΩ) |
| $V_{DD2}$ | 18 | 5 V supply for input comparator |
| RX0, RX1 | 19, 20 | input from the physical CAN-bus line to the input comparator of the SJA1000; a dominant level will wake up the SJA1000 if sleeping; a dominant level is read, if RX1 is higher than RX0 and vice versa for the recessive level; if the CBP bit (see Table 49) is set in the clock divider register, the CAN input comparator is bypassed to achieve lower internal delays if an external transceiver circuitry is connected to the SJA1000; in this case only RX0 is active; HIGH is interpreted as recessive level and LOW is interpreted as dominant level |
| $V_{SS2}$ | 21 | ground for input comparator |
| $V_{DD1}$ | 22 | 5 V supply for logic circuits |

# SJA1000 e BIU (Bus Interface Unit) con µp della famiglia Intel a 8 bit con core 8088 (8051)

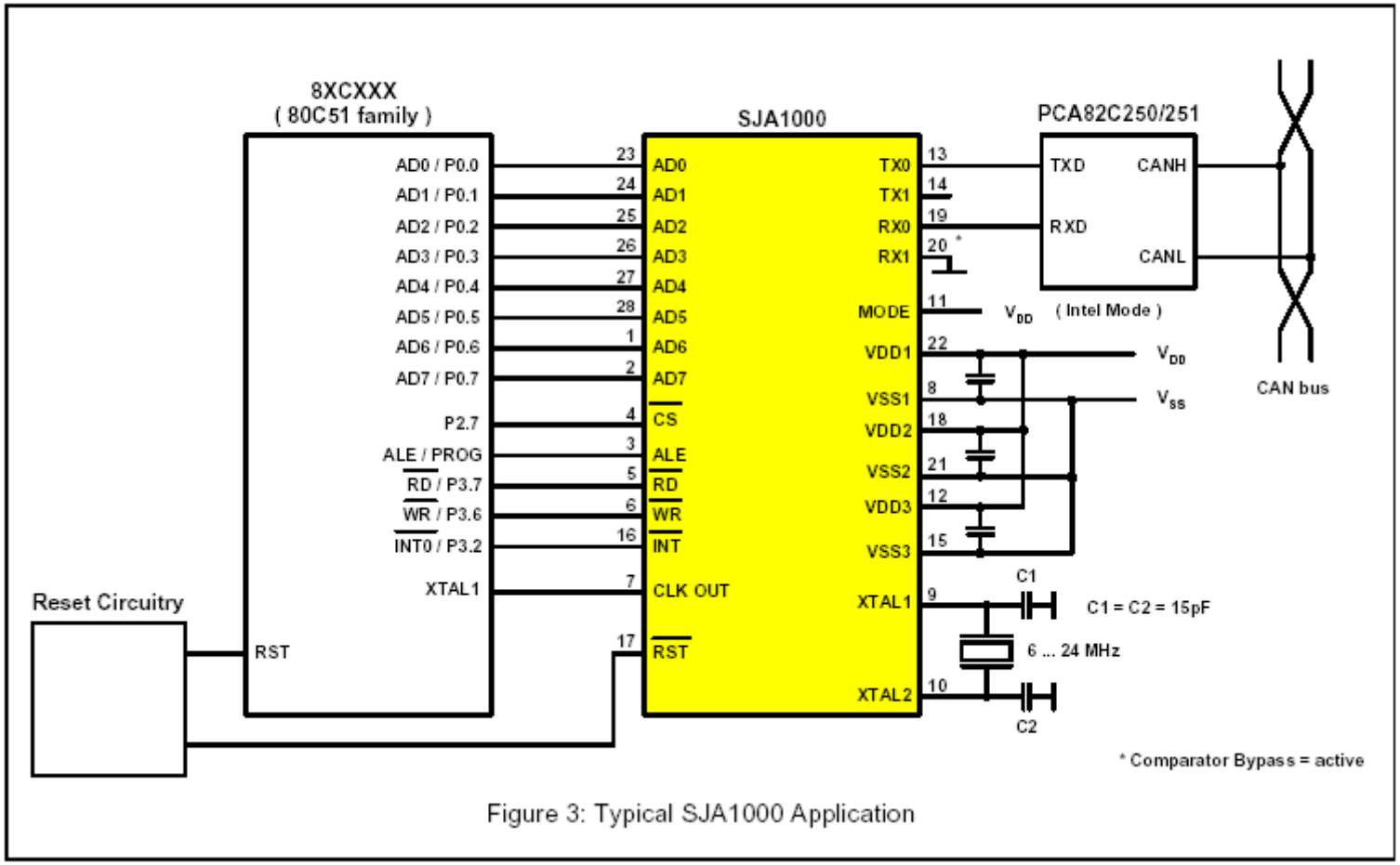
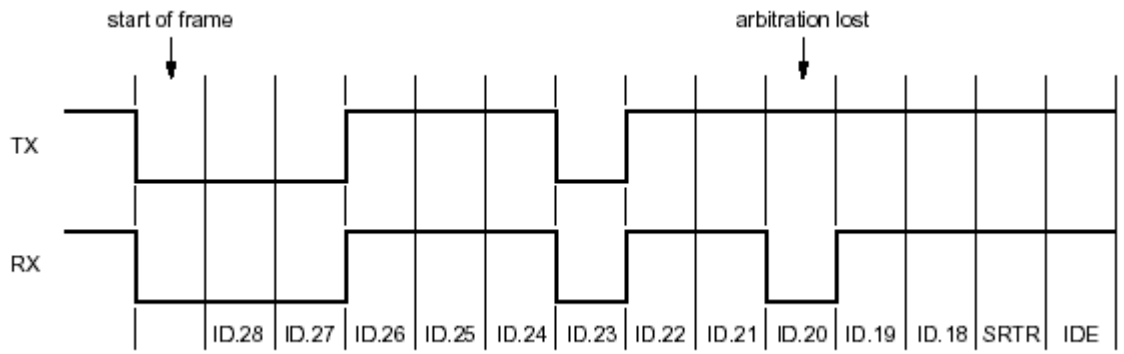
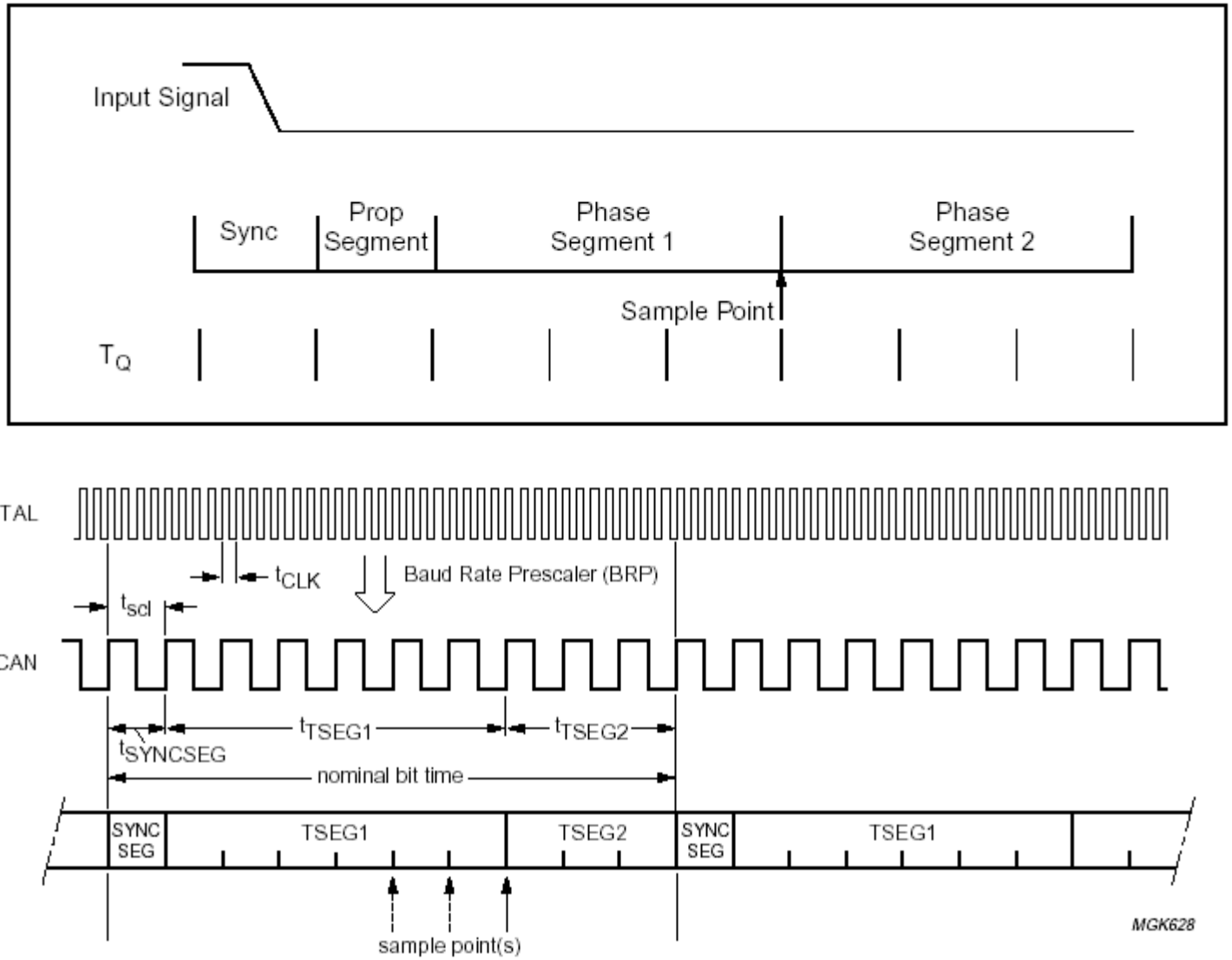



Figure 3: Typical SJA1000 Application

Arbitraggio durante la fase di emissione del Frame ID da parte di due diversi nodi della rete CAN (si suppone l'uso di Extended frames)



# Bit Time partitioning con evidenziazione del sample point



Macchina a stati degli errori

TEC = Transmit Error Counter

REC = Receive Error Counter

Stati di:

Error Active

Error Passive

Bus Off

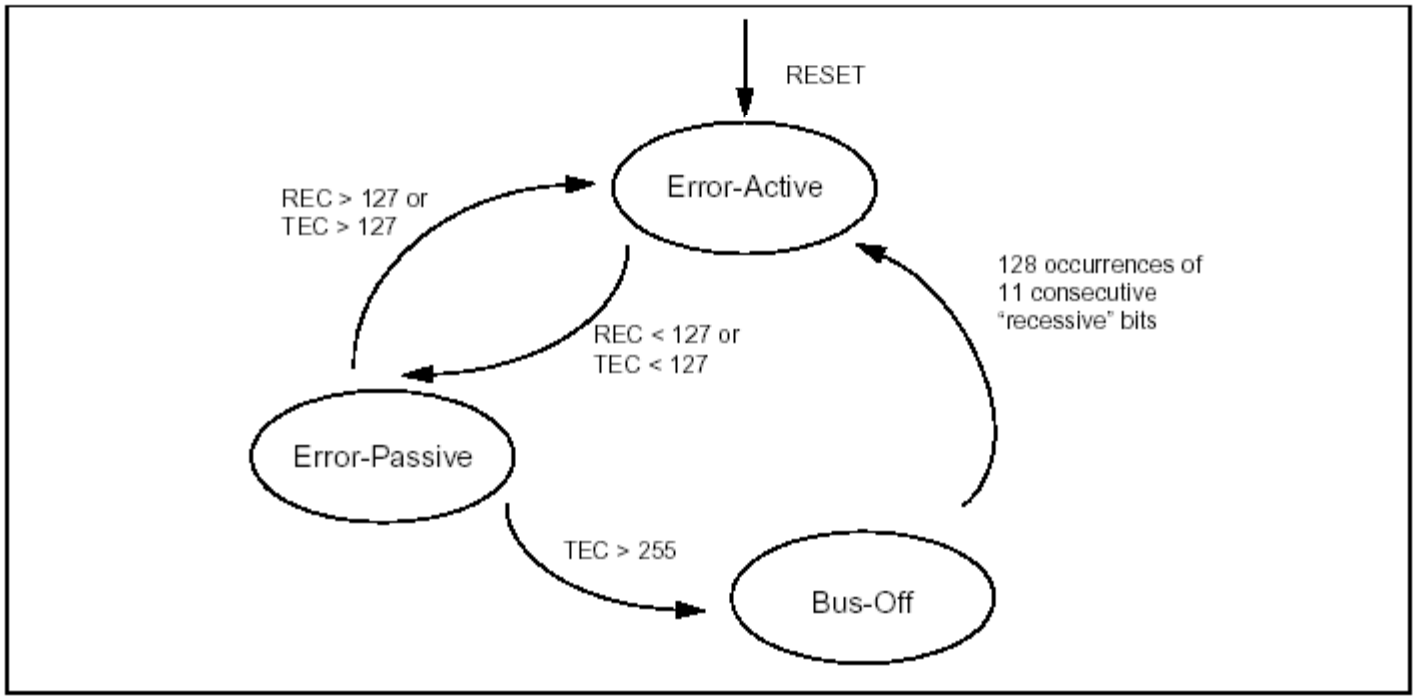
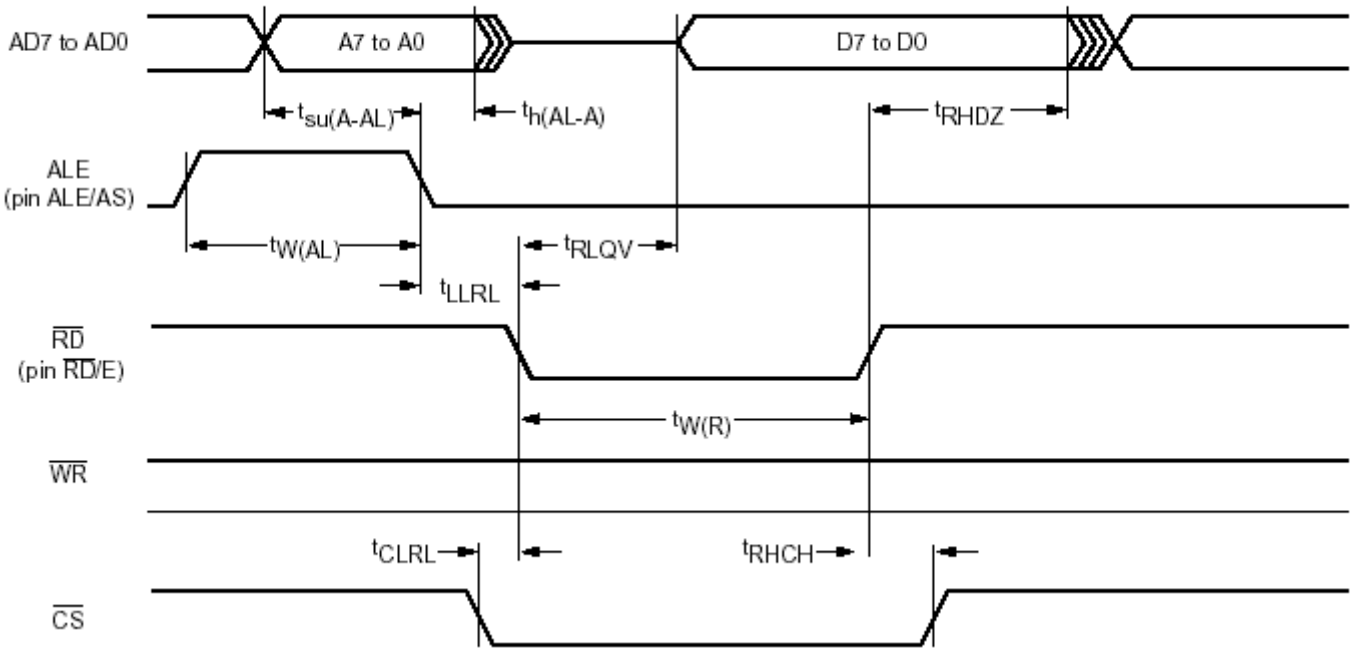
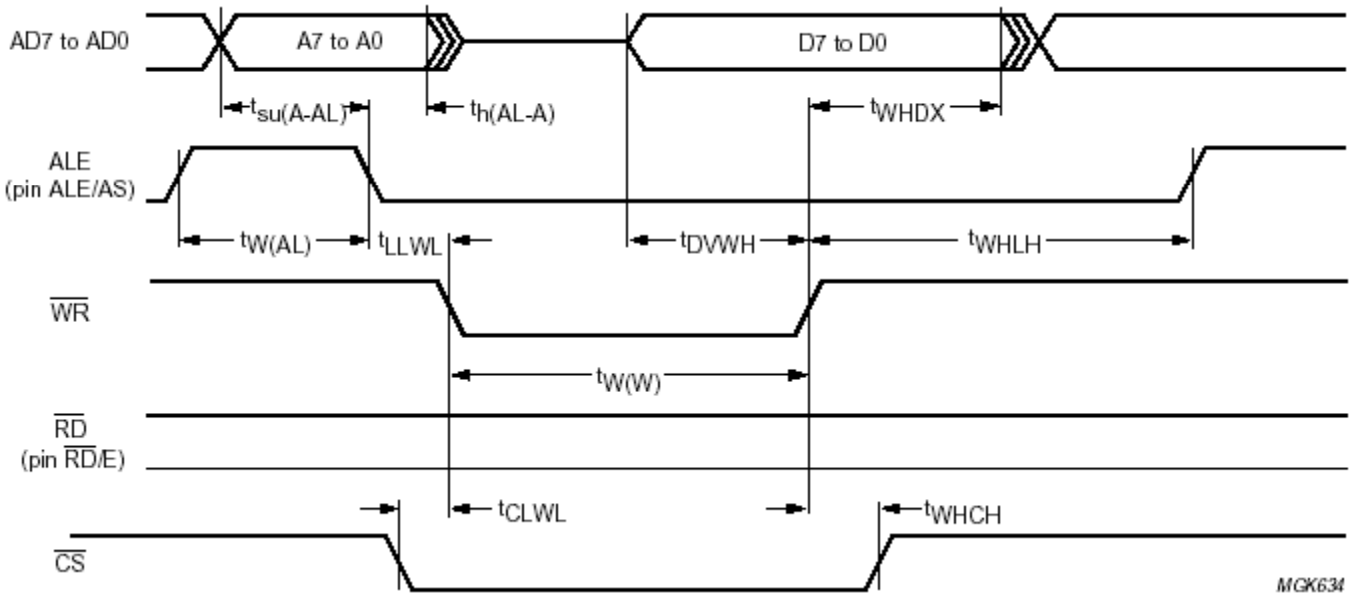



*FIGURE 6-1: Error Modes State Diagram*

# Interfaccia verso la CPU e il Bus di sistema: Ciclo di lettura



# Interfaccia verso la CPU e il Bus di sistema: Ciclo di scrittura



# Interfaccia verso la CPU e il Bus di sistema: Timing dei cicli di lettura e scrittura

| SYMBOL | PARAMETER | CONDITIONS | MIN. | MAX. | UNIT |
|---|---|---|---|---|---|
| $f_{osc}$ | oscillator frequency | | – | 24 | MHz |
| $t_{su(A-AL)}$ | address set-up to ALE/AS LOW | | 8 | – | ns |
| $t_{h(AL-A)}$ | address hold after ALE LOW | | 2 | – | ns |
| $t_{W(AL)}$ | ALE/AS pulse width | | 8 | – | ns |
| $t_{RLQV}$ | $\overline{RD}$ LOW to valid data output | Intel mode | – | 50 | ns |
| $t_{RHDZ}$ | data float after $\overline{RD}$ HIGH | Intel mode | – | 30 | ns |
| $t_{DVWH}$ | input data valid to $\overline{WR}$ HIGH | Intel mode | 8 | – | ns |
| $t_{WHDX}$ | input data hold after $\overline{WR}$ HIGH | Intel mode | 8 | – | ns |
| $t_{WHLH}$ | $\overline{WR}$ HIGH to next ALE HIGH | | 15 | – | ns |
| $t_{LLWL}$ | ALE LOW to $\overline{WR}$ LOW | Intel mode | 10 | – | ns |
| $t_{LLRL}$ | ALE LOW to $\overline{RD}$ LOW | Intel mode | 10 | – | ns |
| $t_{W(W)}$ | $\overline{WR}$ pulse width | Intel mode | 20 | – | ns |
| $t_{W(R)}$ | $\overline{RD}$ pulse width | Intel mode | 40 | – | ns |
| $t_{CLWL}$ | $\overline{CS}$ LOW to $\overline{WR}$ LOW | Intel mode | 0 | – | ns |
| $t_{CLRL}$ | $\overline{CS}$ LOW to $\overline{RD}$ LOW | Intel mode | 0 | – | ns |
| $t_{WHCH}$ | $\overline{WR}$ HIGH to $\overline{CS}$ HIGH | Intel mode | 0 | – | ns |
| $t_{RHCH}$ | $\overline{RD}$ HIGH to $\overline{CS}$ HIGH | Intel mode | 0 | – | ns |
| $t_{W(RST)}$ | $\overline{RST}$ pulse width | | 100 | – | ns |