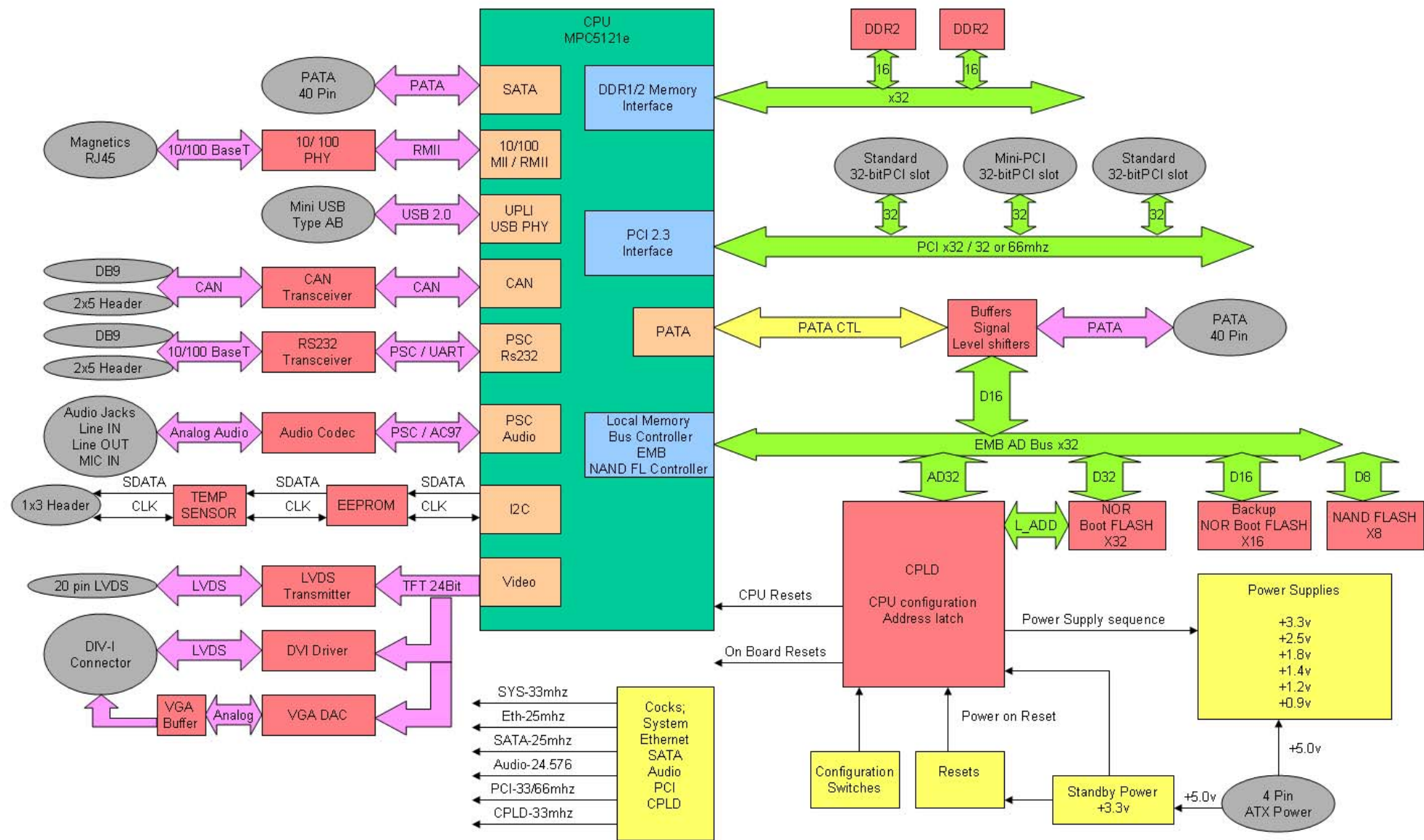
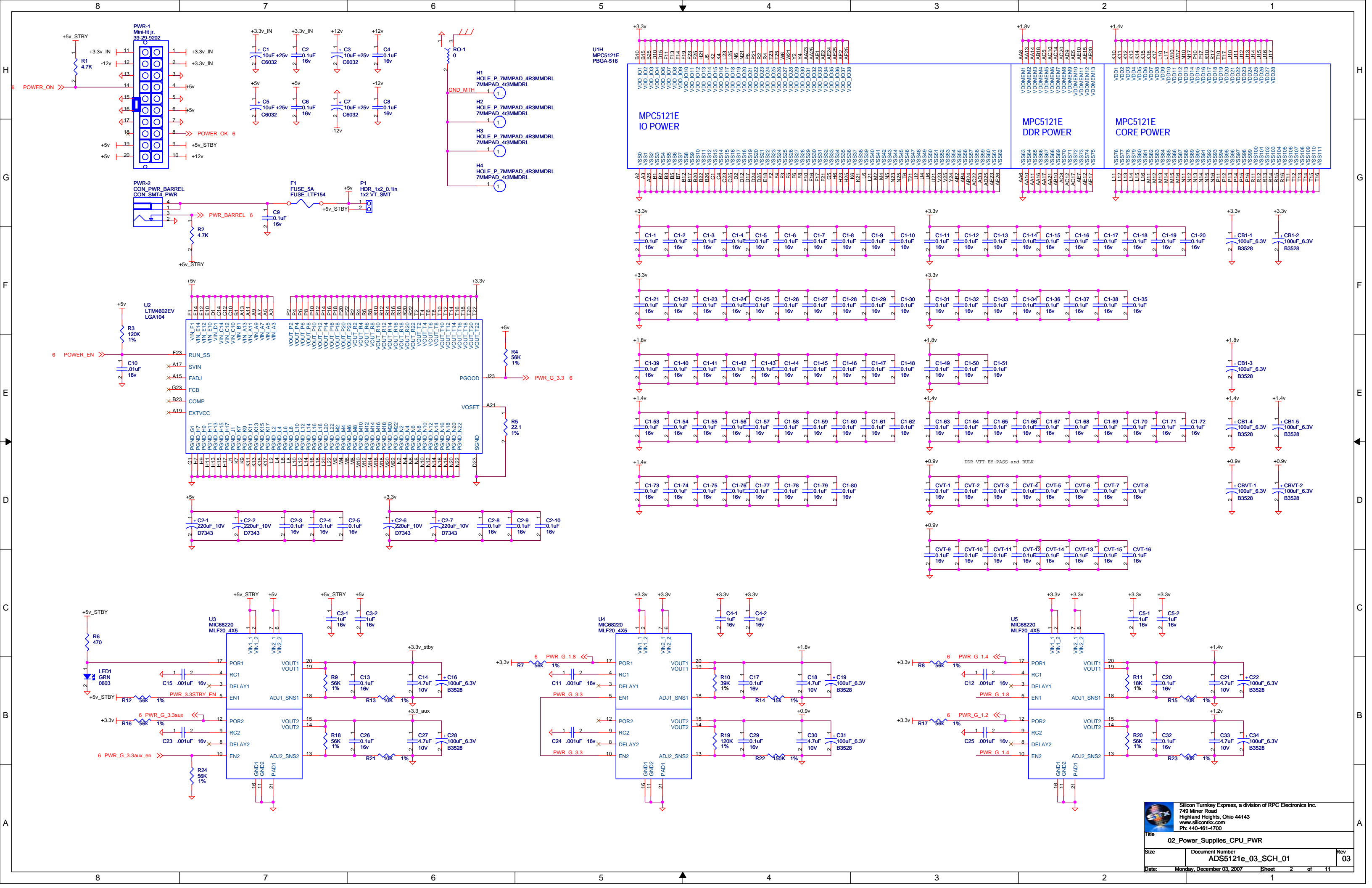
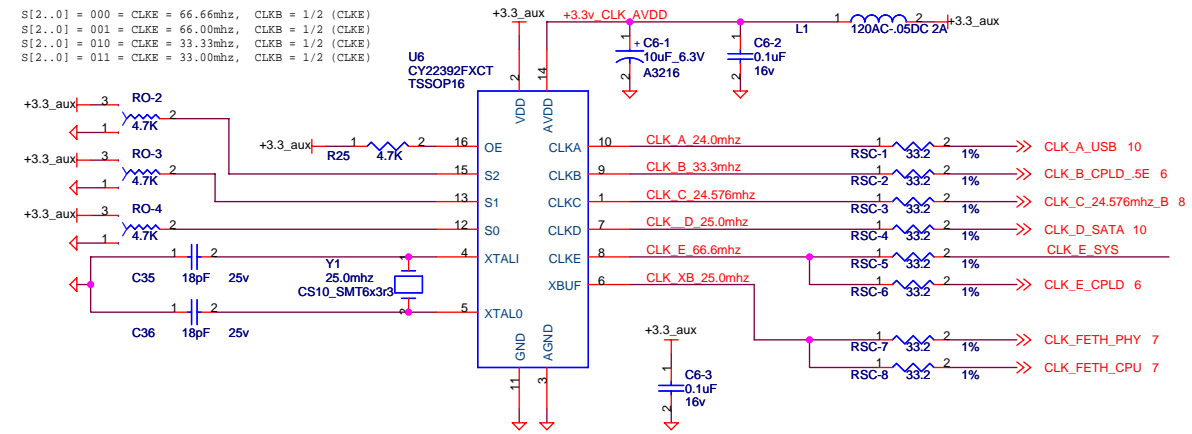


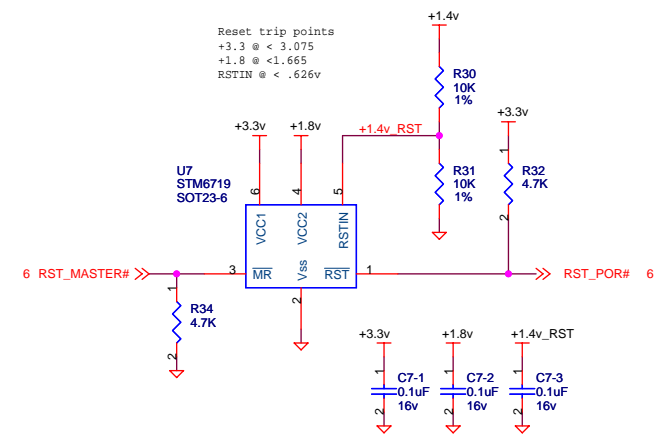
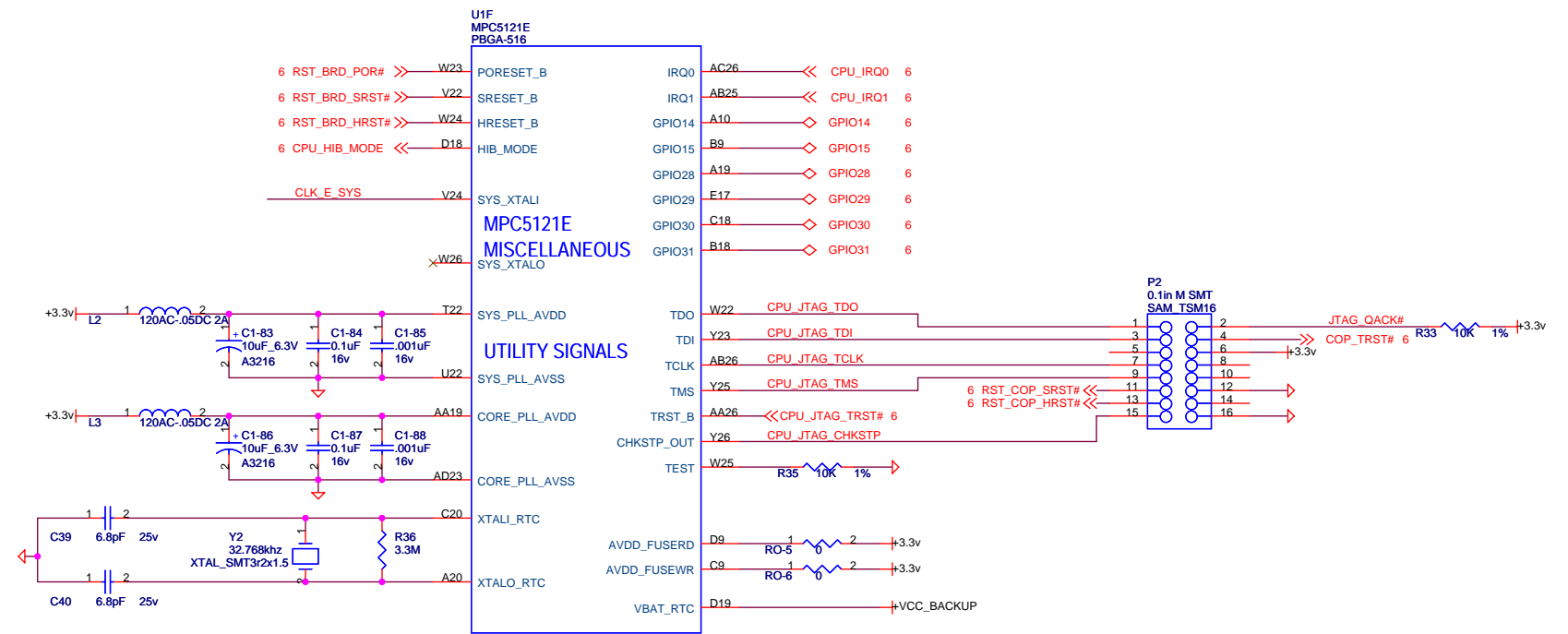
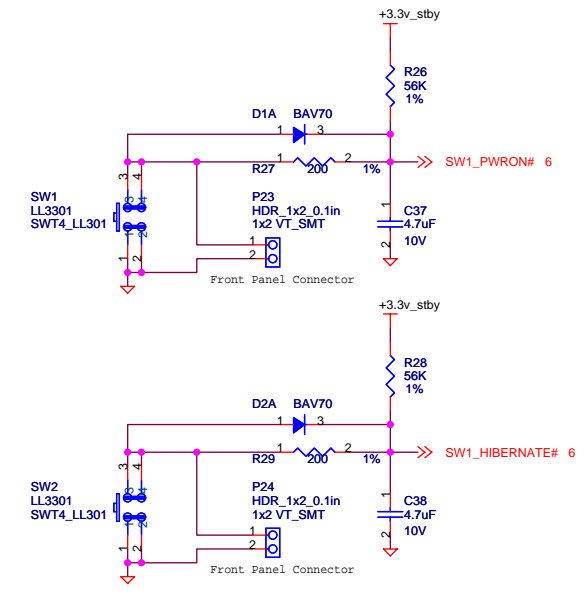
### ADS5121e\_02 BLOCK DIAGRAM

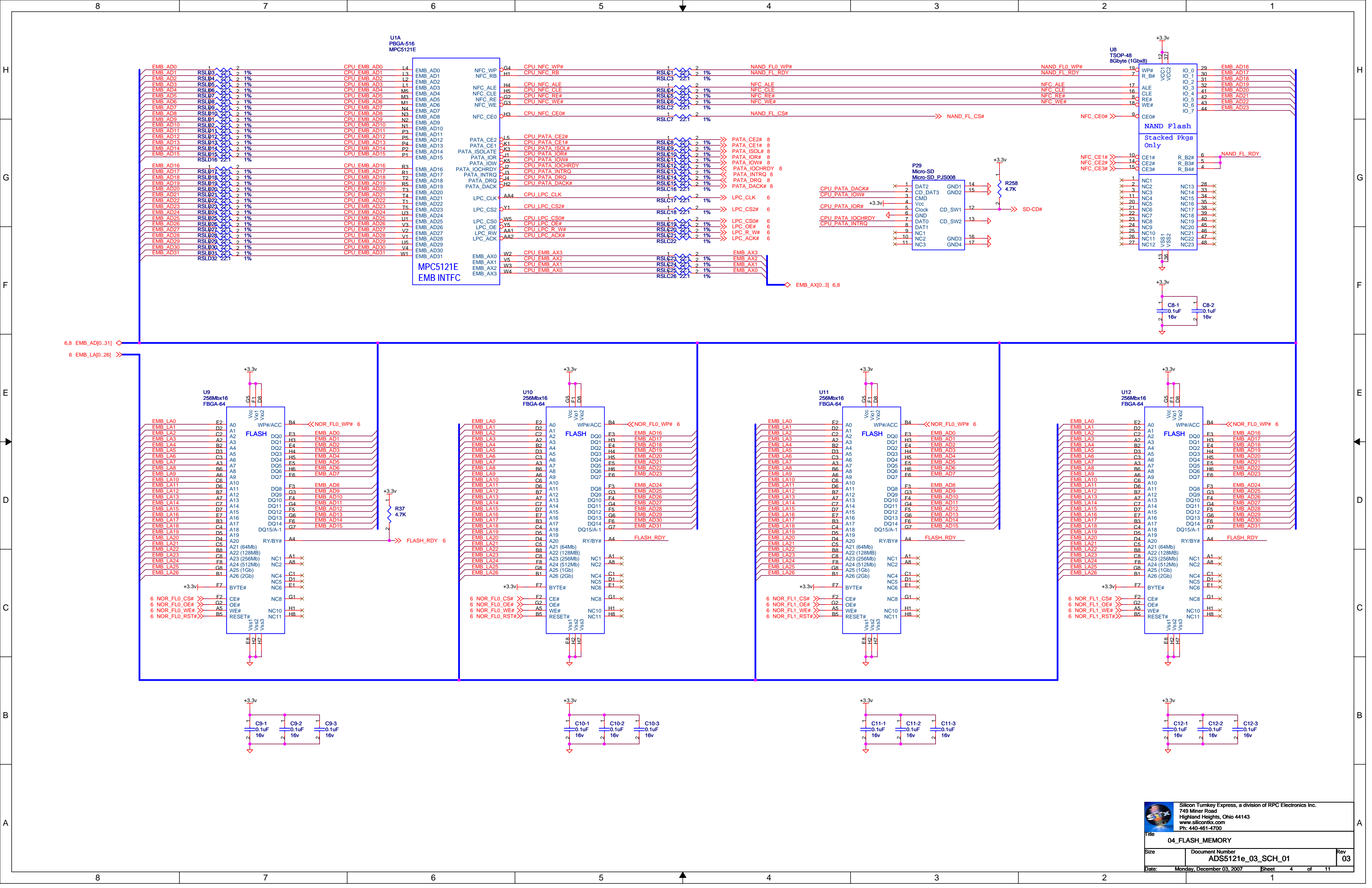




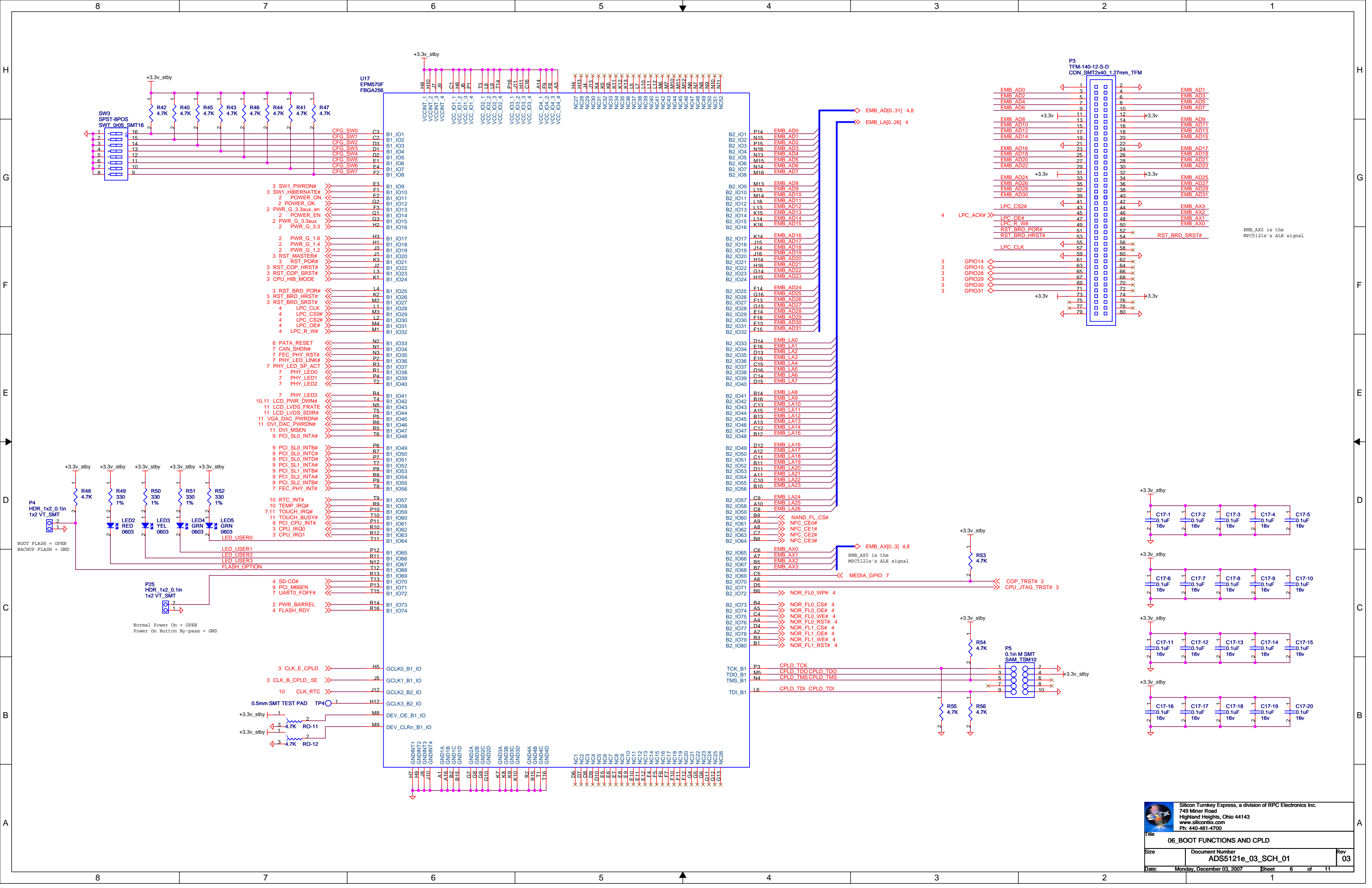


CLOCK RULES:  
 All Clock traces are to be as short as possible  
 CLK\_E\_SYS = CLK\_E\_CPLD  
 CLK\_FETH\_PHY = CLK\_FETH\_CPU

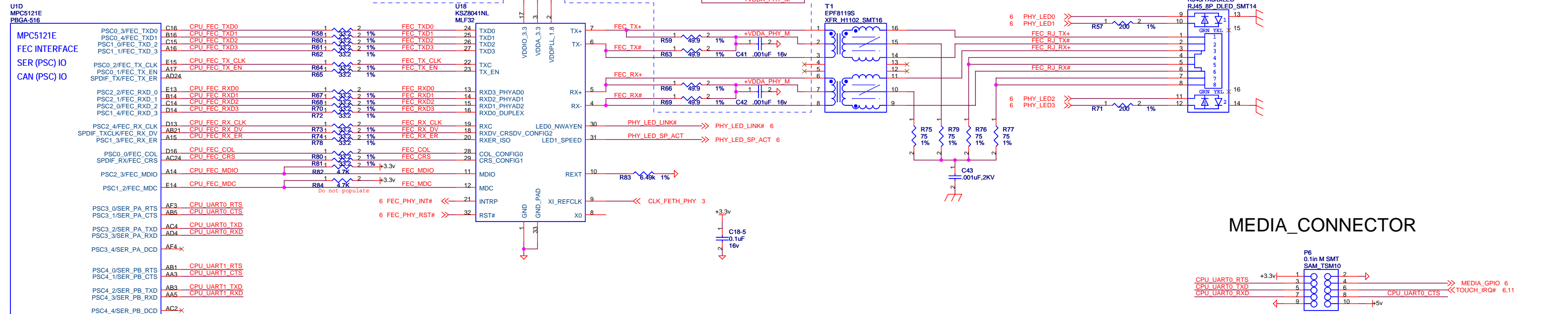




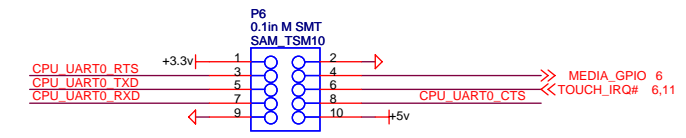




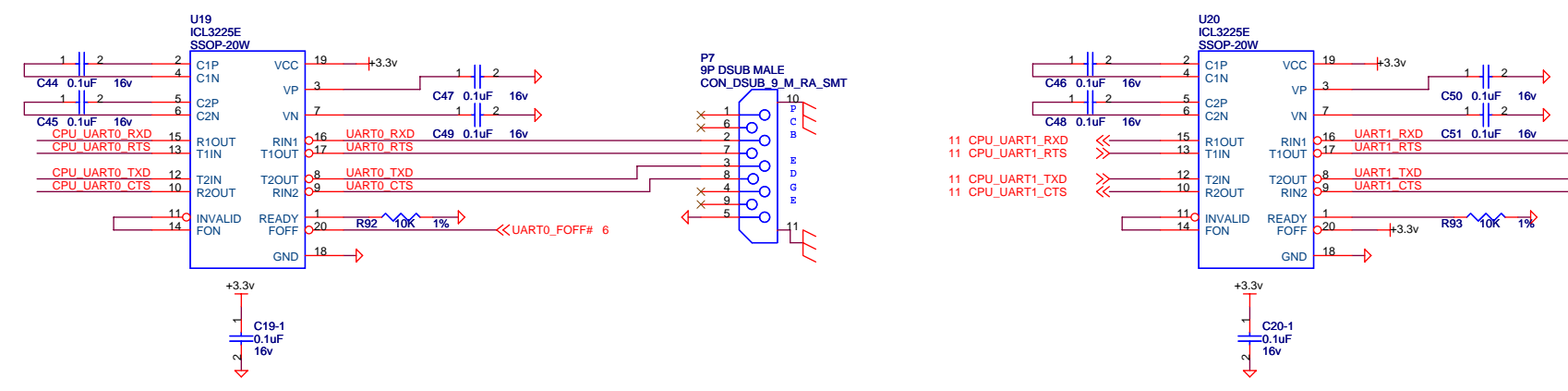
# 10/100 BASET ETHERNET PHY INTERFACE AND CONNECTOR



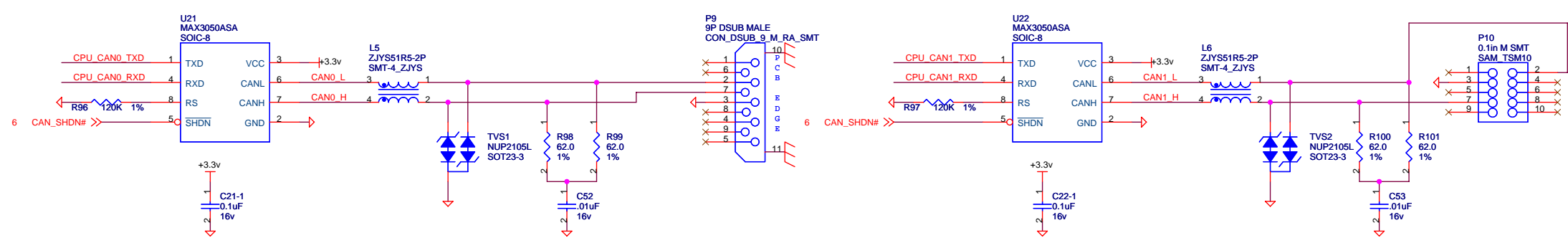
## MEDIA\_CONNECTOR



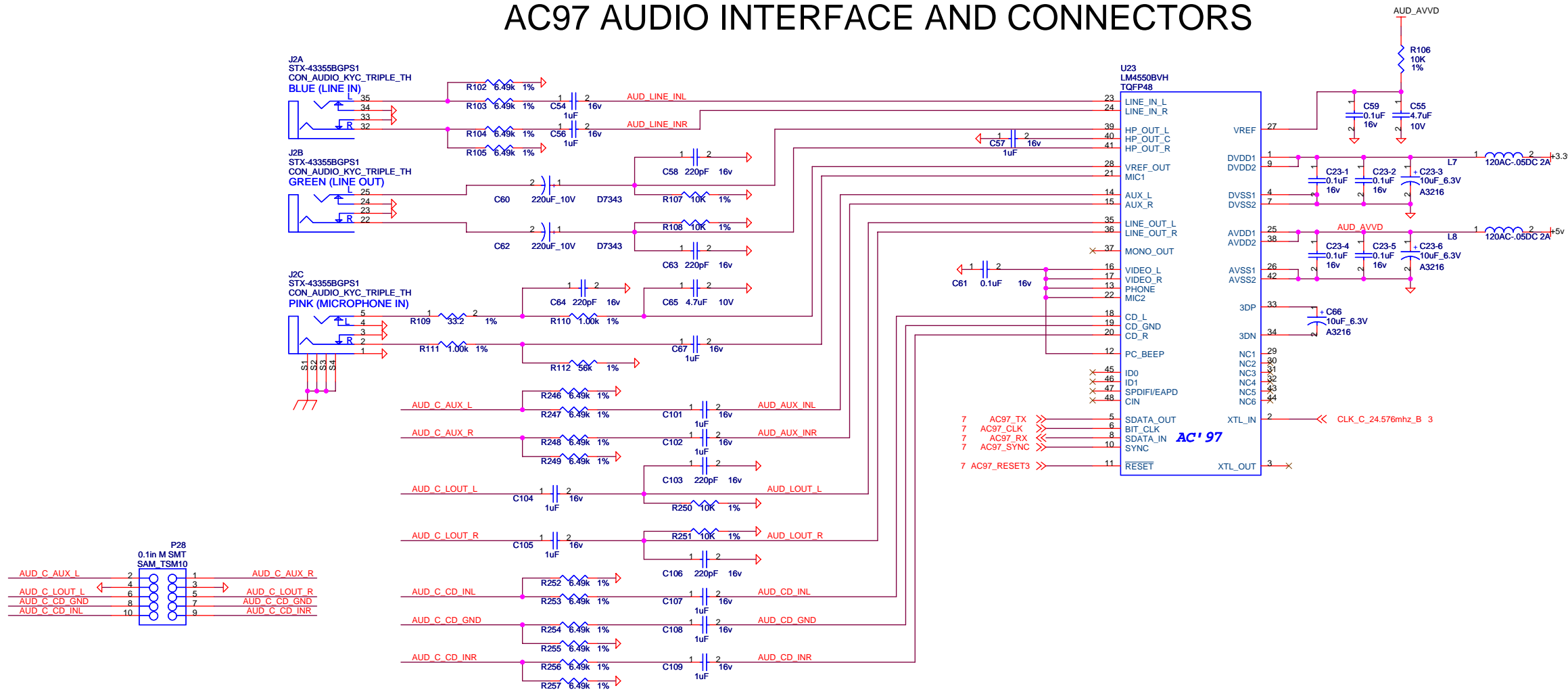
## RS232 UARTS



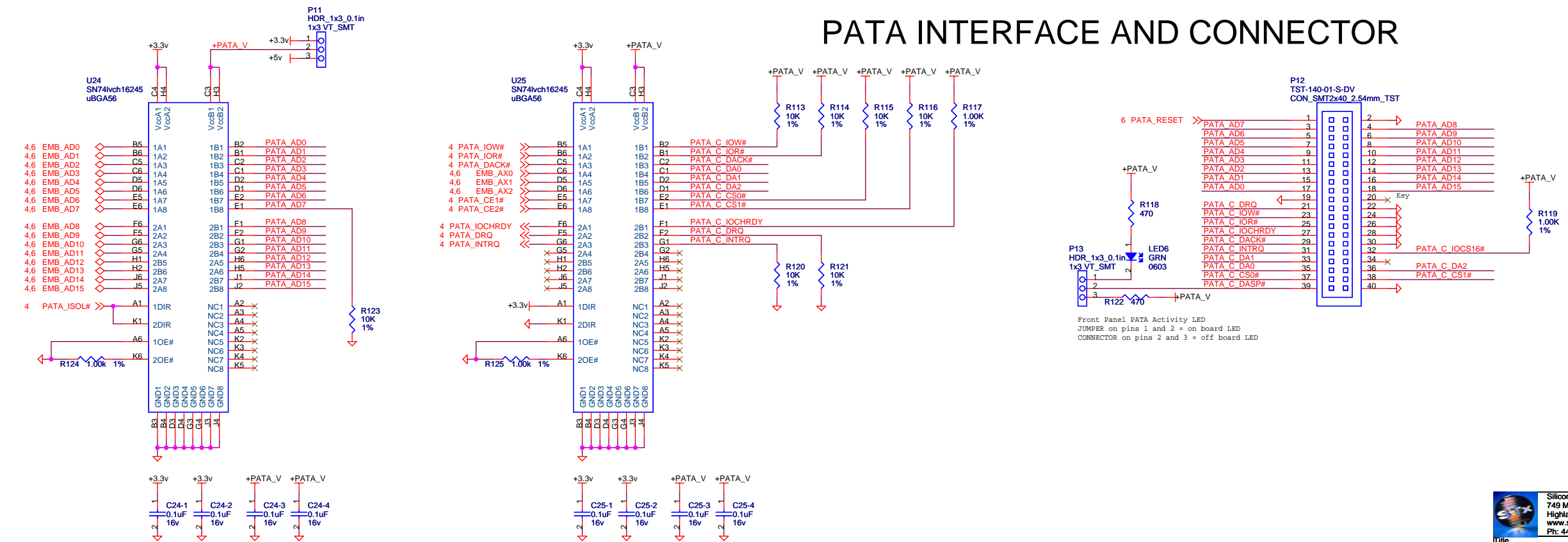
## CAN BUS



# AC97 AUDIO INTERFACE AND CONNECTORS



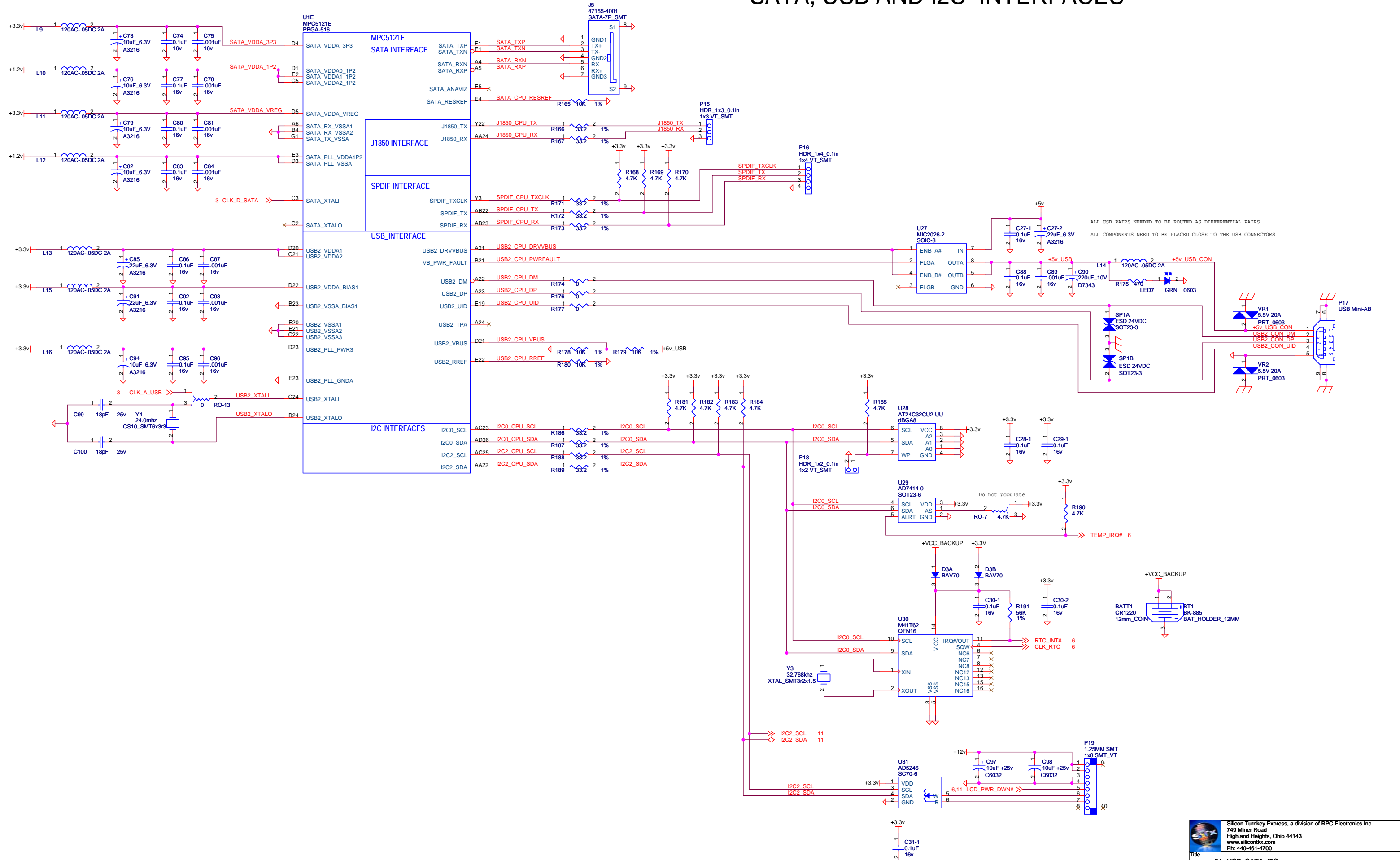
# PATA INTERFACE AND CONNECTOR







# SATA, USB AND I2C INTERFACES



ALL USB PAIRS NEEDED TO BE ROUTED AS DIFFERENTIAL PAIRS  
ALL COMPONENTS NEED TO BE PLACED CLOSE TO THE USB CONNECTORS

