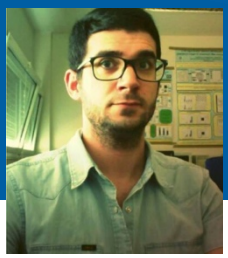

Marco Balboni

Electrical Engineer

Personal Information and Contacts

- **Name** Marco Balboni
- **Birth Date** 07 September 1984
- **Birth Place** Portomaggiore, Ferrara, ITALY.
- **Nationality** Italian.
- **Skype** marcobalboniskype
- **Email** marco.balboni5@unibo.it
  marco.balboni@unife.it

Education

- **Pre-University Studies**
  Scientific Certificate – Italian Secondary School Diploma
  Examination mark: **100/100**

- **Bachelor Degree in Electrical Engineering**
  Thesis: *Implementation of capacitive sensors for smart objects in virtual interaction environments – Tangerine MICREL Cube.*
  Abstract - The Tangerine Smart Micrel Cube (SMCube) is a smart device for Human Computer Interaction (HCI) and a tangible smart object equipped with sensors (digital tri-axes accelerometer as default) and actuators (infrared LEDs, vibro-motors) embedded in a wooden cube. Data from accelerometer is used to locally detect the active face (the one directed upward) and a set of gesture performed by the user. These information are wirelessly sent to a base station for processing. Furthermore, through the LEDs the node can interact with a vision based system in a multi modal activity detection scenario. My thesis project was focused on augmenting the SMCube with capacitive sensors, designing both the hardware faces of the cube and the firmware to control the tactile feedbacks to be used with the accelerometer's ones. The firmware created in assembly (ASM) was needed to program a SoC by Cypress that integrates all the components needed to manage the data from the capacitive sensors.
  Collaboration between MicrelLAB-University of Bologna and University of Ferrara.

- **MSc Degree (2nd level Degree) in Electrical and Telecommuncation Engineering**
  Thesis: *Testing of Energy Harvesting Methods for Body Sensor Networks.*
  Abstract – This thesis project presents an Ultra-Low-Power (ULP) Hybrid Micro Energy Harvester (HMEH) for biomedical application. This architecture uses the inputs of Thermoelectric Generator (TEG) and solar cells. To match different light conditions we equipped our harvester with both indoor and outdoor solar cells, designing also a circuit capable of switching between them. Having two sources overcome the issue of limitation caused by single source harvester but will result in impedance mismatching among the desired sources. The proposed of HMEH architecture consists of a control manager with

Asynchronous Finite State Machine (AFSM) to grab the proper input value, a rectification to convert thermal and photovoltaic cells input from AC to DC, a Maximum Power Point Tracking (MPPT) to achieve maximum power extraction, a boost converter to boost up the input voltage, energy storage to keep the energy and voltage regulator to fix or produce the desired output voltage. The HMEH was modeled, designed and simulated using PSPICE software and then implemented in 0.13 µm CMOS technology. Next, the developed HMEH was coded using Verilog Hardware Description Language (VHDL) and then downloaded to Field Programmable Gate Array (FPGA) for real time implementation, finally considering components on the market and tested it under real operative conditions.
Collaboration between MicrelLAB-University of Bologna and University of Ferrara.

- **Fellow Researcher in MicrelLAB Research Group** at University of Bologna (ITALY)
  Advisor: prof. Luca Benini.
  Hardware extensions for virtualization in embedded systems.
  Abstract – Embedded devices are pervasive in our everyday live and their complexity increases exponentially. Among them, heterogeneous multi-core processors and specific hardware accelerators allow the required computing power while exhibiting a good performance/watt ratio. The flexibility required by them is promoting an application-centric model, which makes future systems face new challenges: Openness (total decoupling from hardware to application software), security, programmability and performance. Virtualization, widely used in the general-purpose computing domain, allows an effective and clean way to isolate applications from hardware, so being suitable to cope with the challenges faced by heterogeneous multi-core embedded systems. However, virtualization on embedded systems is still in its infancy. Their real-time requirements, resource constraints and heterogeneous nature demand for an integral and different approach of the virtualization concept. I took part to the vIrtical project, which aims the vertical and full development of the virtualization concept addressing the specific requirements for effective embedded virtualization. A virtualization-ready SoC platform and the associated programming models were developed, tackling all the system layers: applications, programming model, hypervisor and hardware. This unique integrated approach is able to address the evolution towards heterogeneous multi-cores and even many-cores in embedded systems by focusing not only on the well-known processor virtualization but on the hardware assisted virtualization for the overall SoC. Security and protection, real-time QoS guarantees, reliability, process variation, power savings, and memory coherency were addressed and affected the way the system is virtualized.

- **PhD student in MPSoC Research Group** at University of Ferrara (ITALY)
  Advisor: prof. Davide Bertozzi.
  Modeling and simulation of heterogeneous parallel architectures with interconnect-enabled runtime reconfiguration capability.
  Abstract – Today, multi- and many-core architectures are gaining momentum as a potential source of hardware acceleration, bringing to new challenges for system designers related to both system virtualization and runtime testing. My research activity tackles these challenges exploiting and optimizing the capabilities of reconfiguring the routing function at runtime. My research aims at an optimized usage of parallel hardware resources of the on-chip interconnection network at runtime, to cope with the increased level of resource contention and dynamic application behavior that takes place in the on-chip domain, especially when virtualization is implemented. The key idea consists of partitioning of the array fabrics of homogeneous processor cores and isolation of derived partitions, as means of pursuing the integration of functionality from separate users/devices onto NoC-based many- core processors, while meeting their potentially heterogeneous requirements. Following this trend, the traditional time and space partitioning concept is being extended to parallel hardware platforms to overcome the challenge of using shared (yet modular) resources in applications that are executed concurrently.

- **Hipeac ACACES Summer School 2013**
  Courses taken:
  - *Datacenter power management*, by Anand Sivasubramaniam
  - *Computing system design for reconfigurable platforms*, by Lesley Shannon
  - *Memory hierarchies and their impact on virtualization*, by Alex Garthwaite
  - *Scalable manyCore memory systems*, by Onor Mutlu
  - *Automatic parallelization for computer architects*, by Sam Midkiff

- **High Performance Computing Courses 2014** at CINECA, Bologna (ITALY)
  - *Introduction to Parallel Computing with MPI and OpenMP*.

- **High Performance Computing Courses 2014** at CINECA, Bologna (ITALY)
  - *Introduction to Scientific Programming using GPGPU and CUDA*.

- **High Performance Computing Courses 2015** at CINECA, Bologna (ITALY)
  - *Python for Computational Science*.

Professional Experience

Position: Research Fellow
Period: June 2012 - current
Group: Micrel LAB, **University of Bologna**, Italy
Head: prof. **Luca Benini**
Major depth: virtual prototyping of heterogeneous multi-core architectures, with emphasis on the interconnection network; hardware extensions for virtualization and QoS support in high-end embedded systems.

Position: Post-Doctoral Student in Electrical Engineering
Period: January 2016 - current
Group: MPSoC Research Group, **University of Ferrara**, Italy
Head: prof. **Davide Bertozzi**
Major depth: cross-layer simulation of heterogeneous multi-core architectures, including both transaction-level and RTL-equivalent modeling; design methods for reconfigurable multi-core architectures; hardware extensions of on-chip interconnection networks targeting runtime reconfiguration of the routing function.

Position: Ph.D. in Electrical Engineering
Period: January 2013 - 2015
Group: MPSoC Research Group, **University of Ferrara**, Italy
Head: prof. **Davide Bertozzi**
Major depth: cross-layer simulation of heterogeneous multi-core architectures, including both transaction-level and RTL-equivalent modeling; design methods for reconfigurable multi-core architectures; hardware extensions of on-chip interconnection networks targeting runtime reconfiguration of the routing function.

Position: Intern/Sponsored Student (Hipeac Industrial Grant Winner)
Period: October 2014 – February 2015
Group: **ARM Ltd**, Cambridge (UK) – HPC correlation group.
Head: **Andreas Hansson**; **Secondary Advisors: Andreas Sandberg, Radhika Jagtap**.
Major depth: Memory System and Interconnection modeling: *Transaction-Level Modeling* of next generation cache-coherence interconnects through the **gem5** modeling and simulation environment.

Position: **Teaching Assistant** for the course on *Architectures of Digital Integrated Systems*, **leading the laboratory sessions on *Fundamentals of SystemC Programming***, MSc degree in Electrical Engineering, University of Ferrara, Italy.
Period: January 2013 - current

Position: **Teaching Assistant** for the course on *Electronic Instrumentation and Measurements*, **leading laboratory sessions on *Measurements campaigns on fundamental analog electronic circuits***, MSc degree in Electrical Engineering, University of Ferrara.
Period: March 2015 - current

Position: **System administrator and mantainer** for MPSoC Research Group, University of Ferrara.
Period: January 2013 – current

Position: **Teacher at *Gem5 Boot-Camp***, held in MultithermanLAB at University of Bologna in collaboration with ETH-Zurich (Switzerland), supervised by prof. Luca Benini.
Outlines: gem5 concepts and basic use, gem5 advanced use, gem5 development and design, case study: modeling the Smart Memory Cube (SMC) in gem5.
Period: 24,25,26 March 2015

Fields of Expertise

- ✓ Virtual prototyping of heterogeneous parallel architectures for the high-end embedded computing domain. Key expertise in both transaction-level and RTL-equivalent modeling.
- ✓ Spatial partitioning of multi- and many-core Architectures.
- ✓ Runtime reconfiguration of the system interconnect.
- ✓ Runtime management of general purpose programmable accelerators.

In particular:

- ✓ **Virtual prototyping of heterogeneous parallel computing architectures.**

  High-end embedded systems are becoming widely heterogeneous architectures, including host processors, top-level customized system interconnects, hardware accelerators as well as general purpose manycore programmable accelerators. In order to be able to design such complex architectures, their virtual prototyping is an essential step. I have been involved in the RTL-equivalent modeling of such systems through the SystemC modeling and simulation language, and I am currently involved in the development of a transaction-level modeling framework based on the GEM5 environment. My main focus is on the offload of computation

from a host processor to a manycore accelerator, as well as on the spatial division multiplexing of this latter.

- ✓ **Partitioning and reconfiguration of manycore accelerators.**

  Building on the key expertise on logic-based distributed routing for the interconnect fabric, I am currently fostering new usage models of manycore accelerators, where the computation workload can be effectively shared among multiple concurrent applications both in space and in time.

- ✓ **Lifetime-testing**.

  In order to amortize the investment on large manycore systems, their graceful degradation over time should be enforced. In this direction, I am investigating new methods for built-in self-testing of such systems, centered around the self-testing capability of the interconnect fabric in the presence of background traffic.

- ✓ **Programming Model and Runtime management of heterogeneous systems.**

  I am actively involved in addressing the lack of a standard parallel programming method for MPSoCs. In this respect, I am contributing to the runtime support infrastructure for OpenMP for a non-cache-coherent distributed memory MPSoC. This includes specific extensions to the OpenMP programming model that leverage explicit management of the memory hierarchy.

- ✓ **Virtualization of embedded systems.**

  Adding a hypervisor to an embedded system adds flexibility and higher-layer capabilities, morphing the device into a new class of systems. I am addressing the distinctive attributes of embedded virtualization (efficiency, security, isolation, communication, real-time capabilities) by carefully engineering the hardware support for them and the hardware-software interface.

- ✓ **Emerging interconnect technologies and system architectures.**

  Although structured into on-chip networks, electrical interconnects are running out-of-steam for high-end applications. Optical links and networks are a promising alternative to deliver unprecedented bandwidth densities at better energy-per-bit. I am actively involved to foster photonic integration of manycore systems, with an emphasis on the system-ability of optical interconnect technology, and their system-level modeling.

Partecipation in Research Projects

- **Project: vIrtical,** SW/HW extensions for virtualized heterogeneous multicore platforms.
  Site: http://www.virtical.eu
  Funding body: Collaborative Project: FP7 -ICT -2011-7
  Duration: 36 months (from 15 July 2011)
  Specification: Objective ICT-2011.3.4 Computing Systems
  Partners: University of Bologna (Italy); University of Ferrara (Italy); Virtual Open Systems Sarl (France); STMicroelectronics Grenoble 2 Sas (France); Technological Educational Institute Of Crete (Greece); Sysgo Ag (Germany); Thales Communications Sas (France); Arm Limited (UK).

- **Project: PHIDIAS,** Ultra-Low-Power Holistic Design for Smart Bio-Signals Computing Platforms.
  Site: http://www.phidiasproject.eu
  Funding body: Collaborative Project: FP7
  Duration: 36 months (from 1 October 2012)
  Partners: University of Bologna (Italy); European Research Services GmbH (Germany); Ecole Polytechnique Fédérale de Lausanne (Switzerland); IMEC-NL (Netherlands).

- **Project: PHOTONICA**, Photonic Interconnect Technology for Chip-Multiprocessor Architectures.
  Site: https://sites.google.com/site/photonicaproject/home
  Funding body: FIRB 2008
  Specification: RBFR08LE6V
  Partners: University of Ferrara (Italy); University of Siena (Italy); University of Bari (Italy); University of Murcia (Spain).

Personal Skills

- **Languages:** English ★★★★☆ (very good)
  French ★★☆☆☆ (basic)
  Italian ★★★★★ (native language)

- **Programming Languages:** SystemC, SystemC-TLM, VHDL, Verilog, MatLAB, C, C++, C#, Java, Python, MPI, OpenMP, Assembly (ASM).

- **Tools:** Gtkwave, GNU Debugger (GDB), ModelSim, Docker, Xilinx ISE, Xilinx Vivado, Xilinx XPS, Cadence OrCAD Suite (Capture, Layout Designer), LABview, Synopsys Design & IC Compiler, Cadence SoC Encounter, MatLAB with Simulink, Octave, Microsoft Office Suite (Word, Excel, PowerPoint, Outlook), iWork Suite (Pages, Numbers, Keynote), LibreOffice Suite, Codesys.

- **Simulators:** VirtualSoC, MPARM, gem5.

- **Boards & FPGAs:** Juno Board, Versatile Express, Xilinx Virtex-7, Zynq-7, Spartan-6.

Other Info

- **Technical leader of the "Research at School" project**, aiming at familiarizing high-school students with the research experience, in order to make education and careers attractive for young people. Pilot experience are underway in the Italian provinces of Ferrara and Ravenna. **Principal Investigator: prof. Davide Bertozzi.**
- **Student member of IEEE**, since 2012.
- **Student member of Hipeac**, since 2012.
- **Reviewer** for international scientific journal and conference papers: DATE 2015, DATE 2016, INA-OCMC 2013, INA-OCMC 2014, INA-OCMC 2015, AISTECS 2016, Design Automation for Embedded Systems (DAEM) 2014, DAEM 2015, Networks-on-Chip Symposium 2014, Journal of Low Power Electronics and Applications 2015, Elsevier Journal of System Architecture, NORCAS 2015.
- **Local Arrangement Chair** for the IEEE/ACM Int. NETWORK-ON-CHIP SYMPOSIUM 2014.
- **Web Chair** of IEEE/ACM Int. Network-on-Chip Symposium 2014, INA-OCMC 2013-2014-2015, AISTECS 2016.

List of Publications (partial)

- **"Optimizing the overhead for network-on-chip routing reconfiguration in parallel multi-core platforms"**
  M. Balboni, F. Trivino, J. Flich, Bertozzi
  Best Poster at ACACES 2013, Hipeac Summer School.

- **"Optimizing the overhead for network-on-chip routing reconfiguration in parallel multi-core platforms"**
  M. Balboni, F. Trivino, J. Flich, Bertozzi
  International Systems.on.Chip (SoC) Symposium 2013.

- **"Augmenting Manycore Programmable Accelerators with Photonic Interconnect Technology for the High-End Embedded Computing Domain"**
  M. Balboni, L. Ramini, H. Fankem Tatenguem, A. Ghiribaldi, M. Ortín-Obón, A. Capotondi, V. Viñals-Yúfera, A. Marongiu, and D. Bertozzi.
  International Networks-on-Chip Symposium (NOCS) 2014.

- **"Partitioning Strategies of Wavelength-Routed Optical Networks-on-Chip for Laser Power Minimization"**
  M. Balboni ,M. Ortín-Obón, L. Ramini, L. Zuolo, N. Maddalena, V. Viñals-Yúfera, and D. Bertozzi.
  II Workshop on Exploiting Silicon Photonics for Energy-Efficient Heterogeneous Parallel Architectures (SiPhotonics), 2015.

- **"Synergistic Use of Multiple On-Chip Networks for Ultra-Low Latency and Scalable Distributed Routing Reconfiguration"**
  M. Balboni, J. Flich and D. Bertozzi

Design Automation and Test in Europe, DATE 2015.

- **"NoC-Centric Partitioning and Reconfiguration Technologies for the Efficient Sharing of General Purpose Programmable Accelerators"**
  M. Balboni, D. Bertozzi
  Design Automation and Test in Europe, DATE 2015, Poster presented at PhD Forum and Best Poster Candidate.

- **"NoC-Centric Partitioning and Reconfiguration Technologies for the Efficient Sharing of Multi-Core Programmable Accelerators"**
  M. Balboni, D. Bertozzi
  International Conference on High Performance Computing & Simulation, HPCS 2015.

- **"Evolutionary vs. Revolutionary Interconnect Technologies for Future Low-Power Multi-Core Systems"**
  G.Miorandi, M. Balboni, L. Ramini, D. Bertozzi
  1st International Workshop on Advanced Interconnect Solutions and Technologies for Emerging Computing Systems, AISTECS 2016.

- **"Populating and Exploring the Design Space of Wavelength-Routed Optical Network-on-Chip Topologies by Leveraging the Add-Drop Filtering Primitive"**
  M. Balboni, M. Tala, D. Bertozzi
  International Networks-on-Chip Symposium (NOCS) 2016.